U.S.N.A. --- Trident Scholar project report; no. 377 (2008)

Investigation of the Current Turn-off Characteristics of a GTO Thyristor in an Inductive Pulse Forming Network

by

Midshipman 1/c Gerald E. Vineyard
United States Naval Academy
Annapolis, Maryland

(signature)

Certification of Adviser(s) Approval

Associate Professor John G. Ciezki
Department of Electrical and Computer Engineering

(signature)

(date)

Assistant Professor Thomas Salem
Department of Electrical and Computer Engineering

(signature)

(date)

Acceptance for the Trident Scholar Committee

Professor Joyce E. Shade
Deputy Director of Research & Scholarship

(signature)

(date)

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 074-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATE COVERED
	2 May 2008	

4. TITLE AND SUBTITLE

Investigation of the Current Turn-off Characteristics of a GTO Thyristor in an Inductive Pulse Forming Network

5. FUNDING NUMBERS

6. AUTHOR(S)

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)		8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)		10. SPONSORING/MONITORING AGENCY REPORT NUMBER
US Naval Academy Annapolis, MD 21402		**Trident Scholar project report no. 377 (2008)**

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT	12b. DISTRIBUTION CODE
This document has been approved for public release; its distribution is UNLIMITED.	

13. ABSTRACT (cont from p. 1) capacity of the GTO thyristors could be increased beyond their turn-off current rating. The project demonstrated that the GTO thyristors were capable of reliably interrupting twice their nominal turn-off current rating. Furthermore, the project showed that the turn-off speed of the GTO thyristors is dependent upon the amount of gate current used to turn off the GTO thyristors. The GTO thyristors that were turned off using larger gate currents were able to interrupt higher levels of current and turn off faster than the GTO thyristors that were turned off using smaller gate currents. This research project directly complements current and future Department of Defense (DOD) work being performed on railgun pulse power systems. Inductive power supplies may provide a solution to the energy density requirements of the next generation of electric weapon systems. The experimental results of this investigation demonstrate that GTO thyristors can be used in inductive pulse power supplies to safely interrupt significantly more current than they are nominally rated to turn off.

14. SUBJECT TERMS	15. NUMBER OF PAGES
Gate Turn Off Thyristor, Maximum Interruptible Current, Inductive Turn-off, Pulse Power Supply	**110**
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT

ABSTRACT

The research project involved an investigation of the current interruption capability of Gate Turn Off (GTO) thyristors. Specifically, the project examined factors that had the potential to increase the amount of current that could safely be turned off by a GTO thyristor. During the course of the project, a series of GTO thyristors were used in an inductive pulse forming circuit to interrupt varying amounts of current. The primary objective of the research was to determine how the control current used to turn off the GTO thyristors affected their current interruption capability.

The initial part of the research project involved designing and building the experimental apparatus required to test the inductive turn-off characteristics of the GTO thyristors. Fundamentally, the test circuit consisted of a high-voltage capacitor bank, a wire-wound inductor, the GTO thyristor with its associated control circuitry, and instrumentation to measure the voltages and currents in the circuit. The capacitor bank supplied the energy for each current pulse while the inductor, hand wound using a polyvinylchloride (PVC) core and a length of magnet wire, controlled the shape and duration of the current pulses; the control circuitry determined the timing of the current pulses used to turn the GTO thyristor on and off.

The test circuit utilized a conventional H-bridge driver to control the turn on and turn off of the GTO thyristor. Each leg of the H-bridge was connected to a dedicated capacitor bank that supplied the energy for the turn-on and turn-off gate current pulses. The H-bridge allowed the shape and magnitude of the turn-off gate current pulse to be easily adjusted. The amount of gate turn-off current was adjusted throughout the experiment to determine if the current interruption capacity of the GTO thyristors could be increased beyond their turn-off current rating.

The project demonstrated that the GTO thyristors were capable of reliably interrupting twice their nominal turn-off current rating. Furthermore, the project showed that the turn-off speed of the GTO thyristors is dependent upon the amount of gate current used to turn off the GTO thyristors. The GTO thyristors that were turned off using larger gate currents were able to interrupt higher levels of current and turn off faster than the GTO thyristors that were turned off using smaller gate currents.

This research project directly complements current and future Department of Defense (DOD) work being performed on railgun pulse power systems. Inductive power supplies may provide a solution to the energy density requirements of the next generation of electric weapon systems. The experimental results of this investigation demonstrate that GTO thyristors can be used in inductive pulse power supplies to safely interrupt significantly more current than they are nominally rated to turn off.

KEYWORDS: Gate Turn Off Thyristor, Maximum Interruptible Current, Inductive Turn-off, Pulse Power Supply

ACKNOWLEDGEMENTS

First, I would like to thank my advisors, Dr. John Ciezki and Dr. Thomas Salem whose expertise, guidance, and enthusiasm were essential to the completion of this project.

Second, I would like to thank CAPT (sel) Lynn J. Petersen USN and the Office of Naval Research (ONR) Ship Systems and Engineering Division, (ONR 331) Advanced Naval Power Systems program for providing the financial support for this project.

Third, I would like to thank the laboratory technicians and support staff of the Electrical Engineering Department who patiently worked to supply the parts and materials that were needed to complete this project. Without their patience, dedication, and understanding I would never have finished this project.

Finally, I would like to thank the Trident Scholarship Committee for giving me the opportunity to conduct this research project and for providing invaluable assistance with completion of this report.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF EQUATIONS

GLOSSARY OF TERMS

Anode Current: Electric current flowing from the anode terminal to the cathode terminal of the Gate Turn Off (GTO) thyristor.

Anode Voltage: The difference in voltage potential between the anode terminal and the cathode terminal of the GTO thyristor.

Gate Current: Electric current flowing from the gate terminal to the cathode terminal of the GTO thyristor; used to turn the GTO thyristor on and off.

Gate Voltage: The difference in voltage potential between the gate terminal and the cathode terminal of the GTO thyristor.

Gate Driver: A circuit connected to the gate and cathode terminals of the GTO thyristor that generates the short duration current pulses required to turn the GTO thyristor on and off.

Gate Turn Off (GTO) Thyristor: A current controlled semiconductor switch designed for high power applications; commonly used as an "opening switch" to interrupt (turn off) current. Gate Turn Off Thyristors are sometimes referred to simply as GTOs.

H-Bridge: A circuit topology that can generate current flow in either direction along a circuit path.

Holding Current: The minimum anode current required to maintain a GTO thyristor in its conducting state. When the anode current drops below the holding current, the GTO thyristor will turn off.

Latching Current: The minimum anode current required for the device to turn on. If the anode current is less than the latching current during the turn-on gate pulse, then the the GTO thyristor will not turn on.

Maximum Interruptible Current: The maximum amount of anode current that a GTO thyristor is rated to turn off. If the anode current exceeds the maximum interruptible current during turn-off, then the GTO thyristor is likely to fail.

Maximum Surge Current: The maximum amount of anode current that a GTO thyristor is rated to conduct. If the anode current exceeds the maximum surge current at any point, then the GTO thyristor is likely to fail.

Metal Oxide Silicon Field Effect Transistor (MOSFET): A voltage controlled semiconductor switch that can be used like a transistor but for high power applications.

Opening Switch: A switch whose primary function is to turn off and interrupt the flow of current. Opening switches are vital to the operation of inductor-based railgun power sources.

Pulse Forming Network (PFN): A circuit that uses energy storage components such as inductors and capacitors to generate short duration, high current pulses. Typical PFNs incorporate multiple storage elements that are discharged in sequence to generate the overall current pulse.

Pulsed Power Source: An electrical system designed to store energy over a long charge time and rapidly discharge the energy in a high current pulse. Pulse Power Sources allow power supplies with low average power capability to drive applications requiring high instantaneous power levels

Railgun: A device designed to launch projectiles using electromagnetic force. Railguns incorporate a pair of conducting rails and a large current pulse to accelerate projectiles. The projectile slides between the rails and allows current to flow down one rail, through the projectile, and back along the other rail. The current in the rails generates a magnetic field that interacts with the current in the projectile to force the projectile down the rails.

Repetitive Peak Off-state Voltage: The maximum amount of voltage that the GTO thyristor is designed to block when the GTO is not conducting (i.e. "off"). If the anode voltage exceeds the Peak Off-state Voltage at any point then the GTO thyristor will fail.

Safe Operating Area (SOA): The range of anode current and gate current values over which the GTO thyristor can operate without failing. The GTO thyristor has a different maximum interruptible current depending upon how much gate current is used to turn off the device.

Snubber: A collection of components designed to protect the GTO thyristor during turn-off. Snubbers generally consist of a resistor, a capacitor, and a diode; they are designed to limit the rate at which the anode voltage can rise during device turn-off.

Stray Inductance: Extra inductance found in any complete path (loop) in a circuit due to the surface area enclosed by the loop. Stray inductance becomes an issue in circuit paths where the current changes abruptly because it causes large voltage spikes.

1 INTRODUCTION

Recent research efforts focused on increasing the energy storage and power output capacity of pulse power sources have demonstrated that certain semiconductor switches can be used to interrupt (turn off) significantly more current than they are normally designed to turn off. Researchers at the Institute for Advanced Technology (IAT) at the University of Texas in Austin have found that the Gate Turn Off (GTO) thyristor can be used in some railgun pulsed power sources to interrupt more than twice the amount of current that it is normally designed to interrupt. It may be possible to construct more energy dense pulsed power sources, particularly for railgun systems, if the factors responsible for increasing the current interruption capacity of the GTO thyristors can be identified and exploited.

The Department of Defense (DOD) is researching railgun technology to develop operational weapons for use by the Navy and the Army. The notional railgun weapon system currently under development for the Navy will significantly improve the Naval Surface Fire Support (NSFS) and Naval Gunfire Support (NGFS) capability of future surface ships. Such a shipboard system has the potential to fire projectiles on the order of 20kg at muzzle velocities greater than 2500mps (greater than mach 7) and will be able to effectively reach targets at ranges in excess of 200nm.[1] In comparison, the Mk 45 5-inch deck gun that the Navy currently employs fires a high-explosive 32kg projectile at a maximum muzzle velocity of 808mps (using standard Mk 67 charge) and has a maximum effective range of approximately 13nm.[2] The United States Army is working to field a railgun system for its next series of future combat systems.

One of the many technical impediments to achieving an operational railgun weapon system is the development of energy-dense pulsed power sources. Such sources must be small enough to fit into the gun enclosure while still satisfying the significant energy storage requirements. Additionally, the pulsed power source for the Army railgun system will need to meet the weight limitations of a tank-mounted railgun system. At present, high energy pulsed power sources are almost exclusively implemented using large banks of capacitors. Unfortunately, despite recent advances in capacitor technology, these capacitor-based sources currently do not provide high enough energy density for practical platform implementation.

Although continuing to focus on capacitive-based pulse forming networks, the Navy has begun to explore other types of pulse power sources. One potential alternative to capacitive energy storage are inductive-based pulse forming networks. Inductive pulse forming networks utilize large inductors to store up energy and have the potential, especially with recent advances in superconductor technology, to satisfy the energy density requirements of a shipboard railgun weapon system.[3] Unfortunately, significant advances in semiconductor switching technology are required in order to realize practical inductive pulse forming networks.

Within the last two years, researchers at IAT have constructed and tested a railgun launcher that used an inductive pulse forming network as its pulsed power source. The inductive pulse forming network was discharged into the railgun launcher using a GTO thyristor. During testing of the railgun system, the researchers discovered that the GTO was able to interrupt (turn off) more than twice the current that it was nominally rated to interrupt. However, full characterization of the GTO thyristor to fully explain this phenomenon was outside the scope of their research effort.

The goal of this project was to investigate the turn-off switching characteristics of GTO thyristors in an inductive pulse forming network in order to identify potential mechanisms for increasing their current interruption capacity. The project examined the maximum interruptible current of GTO thyristors as a function of the gate current used to turn off the GTOs and the amount of snubber capacitance used to protect the GTOs during turn-off. This project yielded insights into the switching behavior of GTO thyristors that may prove useful to future research efforts towards improving the switching performance of GTO thyristors and increasing the energy density of railgun inductive pulsed power sources.

1.1 Background – Inductive Pulse Forming Network

In June of 2005, researchers at the Institute for Advanced Technology, University of Texas at Austin (IAT-UT) constructed a railgun launcher using an inductive-based pulse power source. The power source used a novel circuit topology (referred to as a STRETCH meatgrinder and described in Appendix A) to provide improved power output capacity and energy density over traditional inductive pulsed power supplies.[4] One of the key components of the pulsed

power source was the GTO thyristor that initiated the railgun firing. The total energy capacity of the power source was determined by the amount of current that the GTO thyristor (commonly referred to simply as a GTO) could safely interrupt (turn off). When the researchers tested the railgun system they discovered that the GTOs could safely turn off more than twice their rated maximum interruptible current.

Fundamentally, the pulsed power source developed at IAT, shown in Figure 1, is an inductive pulse forming network (PFN) that uses a large inductor to store up the energy for each railgun launch. When the GTO turns on (enters the conduction state), energy is transferred from the DC power supply V1 to the storage inductors L1 and L2. If the GTO switch turns off (enters blocking state) when current is flowing through the inductors, the energy in the inductors discharges into the railgun (modeled here by the inductance and resistance -- L3 and R3 respectively). Additional details regarding the operation of the IAT inductive PFN are provided in Appendix A.

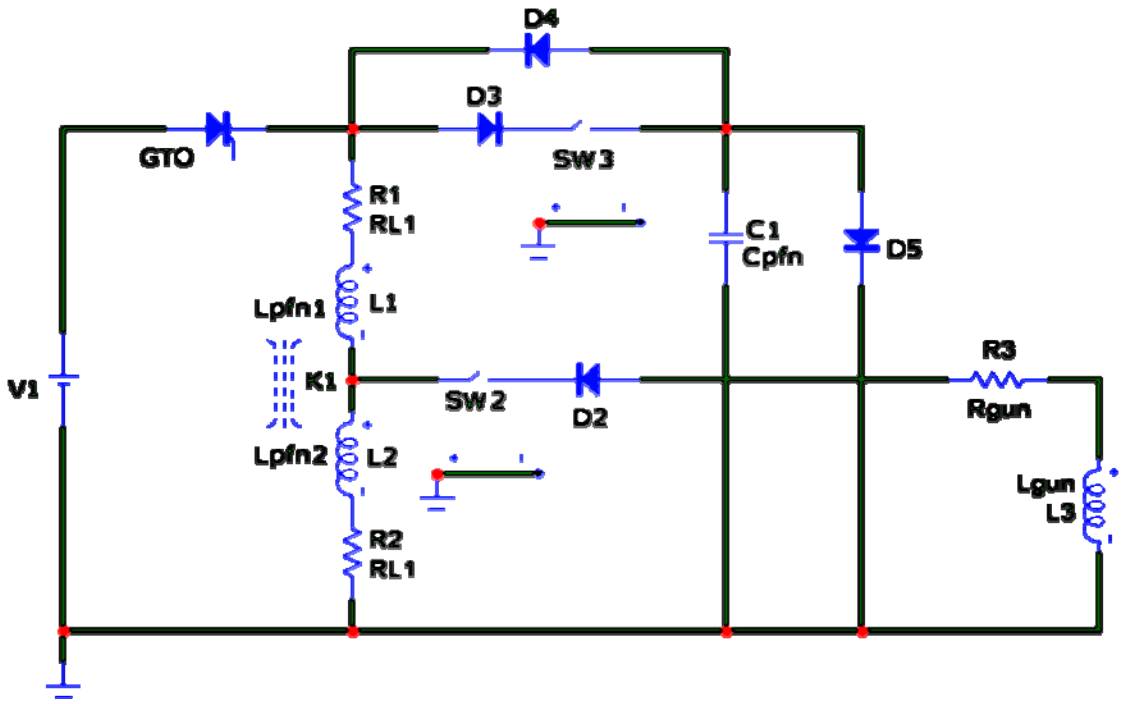


Figure 1: Inductive Pulse Forming Network developed by IAT-UT

The circuit shown above represents the actual inductive PFN that was used to drive a 0.5m demonstration railgun. The opening switch was implemented with a GTO thyristor (Part No. 5SGA 20H2501 from ABB Semiconductor) that was rated to repetitively turn off 3.8 kA and

block up to 4.5kV. However, during testing of the railgun system, the researchers discovered that the GTO thyristors were able to safely interrupt more than 7kA of current.[5] Unfortunately, the researchers did not have the opportunity to fully investigate the turn-off characteristics of the GTO and were unable to determine why the GTOs were able to interrupt more current than they were rated to interrupt. They recommended additional follow-on effort to investigate the GTOs and potentially determine the cause(s) for the increase in current blocking capability.

1.2 Background – Gate Turn Off Thyristor

Gate Turn Off thyristors (commonly referred to simply as GTOs) are solid-state semiconductor switches that are designed for high power switching applications. They have excellent voltage blocking capacity and very low forward conduction drop. They were developed in the 1980s to be one of the first fully controllable semiconductor power switches employing both turn-on and turn-off capability.

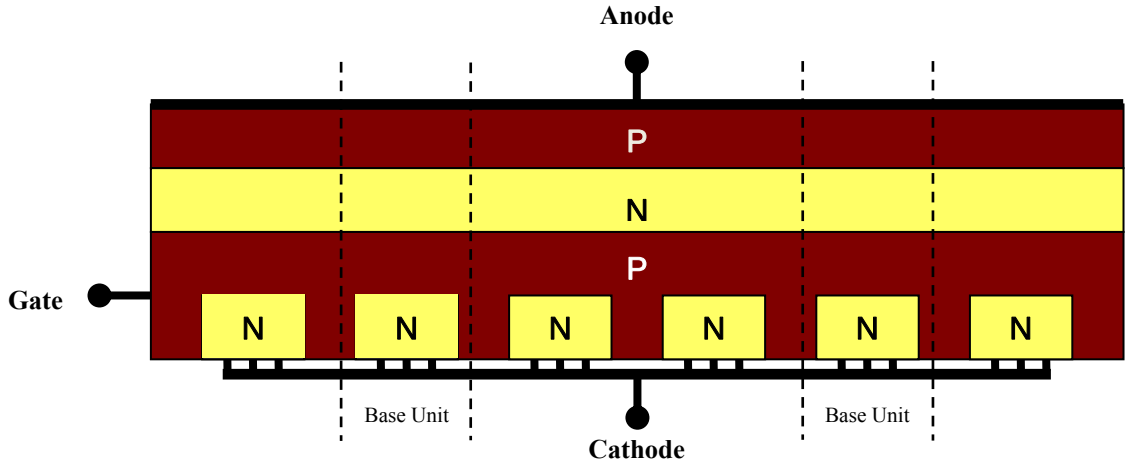


Figure 2: Physical Structure of a GTO Thyristor[6]

Physically, GTO thyristors consist of individual semiconductor base units that are connected together in parallel as shown in Figure 2. Each base unit is comprised of four alternating layers of n-type and p-type semiconductor material and functions like a pair of coupled bipolar junction transistors as shown in Figure 3. The transistor pair consists of a pnp transistor (the top transistor in the figure) coupled to an npn transistor (the bottom transistor in the figure) such that the collector of the pnp transistor connects to the base of the npn transistor and the collector of the npn transistor connects to the base of the pnp transistor. By design, a pnp

transistor will conduct whenever current is pulled from its base and a npn transistor will conduct whenever current is injected into its base. In a GTO thyristor, the current flows along two paths from the anode to cathode; out from the base of the pnp transistor region and into the collector of the npn transistor region and out from the collector of the pnp transistor and into the base of the npn transistor region. This arrangement allows the anode current to continually generate the base currents needed to keep both transistor regions conducting. As long as the anode current remains above the minimum "holding current" for the device, the GTO thyristor will continue conducting even with no current flowing into its gate terminal.[7]

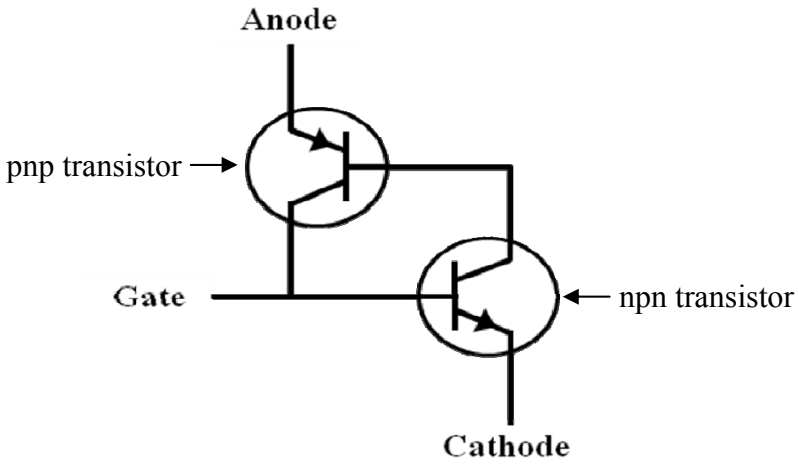


Figure 3: Two Transistor Model of a GTO Thyristor Base Unit

GTO thyristors are current-controlled devices that have two stable operating states, conducting and blocking. Like Silicon Controlled Rectifiers (SCRs), GTO thyristors have excellent voltage blocking and current conducting capabilities and, as described above, do not require a continuous gate current to remain in the conducting state. GTO thyristors are switched between their two stable operating states by applying a current pulse to the gate terminal.

Very little current flows from the anode to cathode of a GTO thyristor that is in the voltage blocking state. Consequently, the gate currents for the transistor regions (npn and pnp) in each base unit of the GTO thyristor are effectively zero and the transistors regions remain in the cutoff mode to block the flow of current. A GTO thyristor in the voltage blocking state behaves like a transistor that is in the cutoff mode. As such, a GTO thyristor in its voltage blocking state can handle abrupt changes in anode to cathode voltage without being unduly damaged.[8]

Once a Gate Turn Off thyristor enters the current conducting state, the anode current continuously regenerates the gate currents of the two transistor regions in each base unit. The base units are designed such that the two transistor regions are easily driven to saturation. As a result, a GTO thyristor in the current conducting state behaves like a forward biased diode. GTO thyristors remain in the current conducting state as long as there is sufficient anode current to keep the two transistor regions saturated.[9] The minimum amount of current needed to maintain current conduction is a physical device property commonly referred to as the "holding current."

Like other thyristors, GTO thyristors are turned on by applying a positive current pulse to the gate terminal. The gate pulse supplies the initial current necessary to drive the two transistor region of each base unit into saturation. The gate pulse first turns on the npn transistor region and allows current to flow out of the gate of the pnp transistor region and into the cathode of the GTO thyristor. The pnp transistor gate current turns on the pnp transistor region and allows current to flow from the anode of the GTO thyristor to the gate of the npn transistor region. The turn-on current pulse has to last long enough to turn on both transistor regions and drive both regions into saturation. Once the device is in the conducting state, the anode current generates the gate currents necessary to keep the transistor regions in each base unit saturated.

GTO thyristors are turned off by applying a negative current pulse to the gate terminal. The turn-off current pulse removes electric charge from semiconductor layers and interrupts the current flow through each base unit. As electric charge is removed from the gate region of each base unit, the flow of current into the gate of the npn transistor regions decreases and the npn transistor region drops out of saturation. When the npn transistor region drops out of saturation, the flow of current from the base of the pnp transistor region suddenly decreases and the pnp transistor region drops out of saturation. The turn-off current pulse has to be large enough to interrupt the current flowing into the base of the npn transistor region. Additionally, the turn-off current pulse has to last long enough for both transistor regions to drop out of saturation and enter the cutoff mode.[10]

Unfortunately, GTO thyristors are very susceptible to damage during the turn-off process. In the current conducting state, the anode current is distributed evenly over all of the base units in the GTO thyristor. During turn off, the base units closest to the gate terminal shut off sooner than the base units farthest from the gate terminal. Consequently, the anode to cathode current is

forced away from the gate terminal into an increasingly smaller area of the GTO until the current is ultimately "pinched off." If the switch does not turn off fast enough, then the GTO can suffer thermal failure in the pinch off regions. Additionally, the GTO can fail if the anode voltage rises too rapidly during switch turn off. When GTOs transition from current conducting to voltage blocking, they pass through an intermediate state in which they do not behave like forward biased diodes or like pnp transistors in cutoff. As a GTO thyristor turns off, the voltage blocking capacity of the device rises as the anode current in the device falls. During this intermediate switching state, the GTO will fail if the anode voltage increases faster than its voltage blocking capability.

There are several ways to prevent failures during the turn-off switching of GTO thyristors. Reducing the turn-off time decreases the likelihood of thermal failure in the pinch off areas. The turn-off time can be decreased to a limited extent by applying a larger current pulse to the gate terminal of the GTO. Controlling the rate of increase in the anode voltage decreases the likelihood of the anode voltage exceeding the voltage blocking capacity of the GTO during turn off. The rate of voltage increase can be limited by placing a snubber circuit across the GTO thyristor as shown in Figure 4.

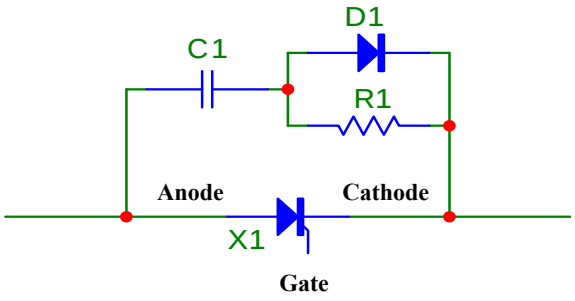


Figure 4: Resistor-Capacitor-Diode (RCD) Turn Off Snubber[11]

When the GTO thyristor is turned off, the anode voltage can only rise as fast as the voltage on the snubber capacitor (C1 in Figure 4). By selecting a large enough snubber capacitor, the rate of anode voltage rise can be maintained within a safe level. The resistor in the snubber network allows the snubber capacitor to discharge through the GTO thyristor when the GTO is turned on. The diode provides a low resistance path to charge up the snubber capacitor during GTO turn off. Essentially, a snubber circuit (the capacitor, diode, and resistor in Figure 4)

provides a low impedance path to filter out the high-frequency (rapidly rising) voltages transients that are generated when the GTO shuts off.

The plot in Figure 5 shows the expected turn-off voltage and current waveforms for a typical GTO thyristor. The top plot shows the anode voltage (solid line) and the anode current (dotted line) during switch turn off. The bottom plot shows the gate-cathode voltage (solid line) and the gate-cathode current (dotted line) during switch turn off. The magnitude of the gate current I_G directly impacts the storage time t_s required to remove enough charge from the gate terminal to begin turning the GTO thyristor off. Once the GTO thyristor begins to turn off, the gate voltage rapidly rises to its maximum value V_G and the anode voltage starts to rise. As the anode voltage V_A nears its final value the anode current begins to decay away as the current through each base unit is pinched off. The amount of current interrupted by the GTO thyristor is known as the anode blocking current I_A.

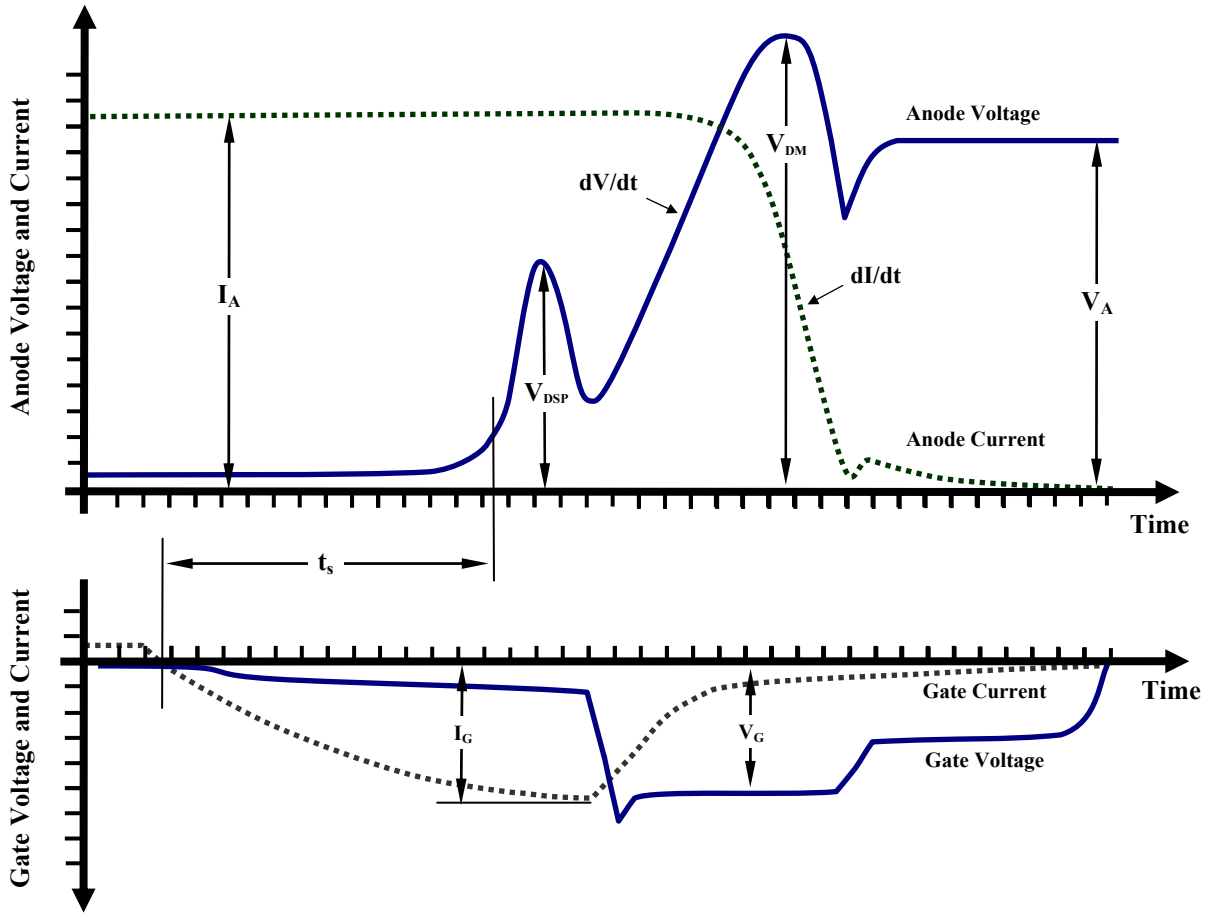


Figure 5: Expected GTO Thyristor Turn-off Waveforms[12]

The anode voltage waveform shown in Figure 5 illustrates the importance of using a snubber circuit to protect a GTO thyristor during turn-off switching. There are two voltage spikes in the anode voltage that can damage or destroy an unprotected GTO thyristor during turn off. The initial spike in anode voltage (V_{DSP}) is caused by stray inductance in the snubber circuit and occurs during the initial surge of current into the snubber circuit when the GTO starts turning off. Once the current in the snubber circuit reaches its peak value, the voltage generated by the stray inductance disappears, allowing the anode voltage to equal the voltage on the snubber capacitor. If the stray inductance of the snubber circuit is too large, then the initial voltage spike V_{DSP} can exceed the blocking voltage of the GTO and cause the device to fail. Figure 6 shows the expected voltage (solid line) and current (dotted line) in a snubber capacitor. Notice that the snubber capacitor voltage does not spike when the GTO first turns off.

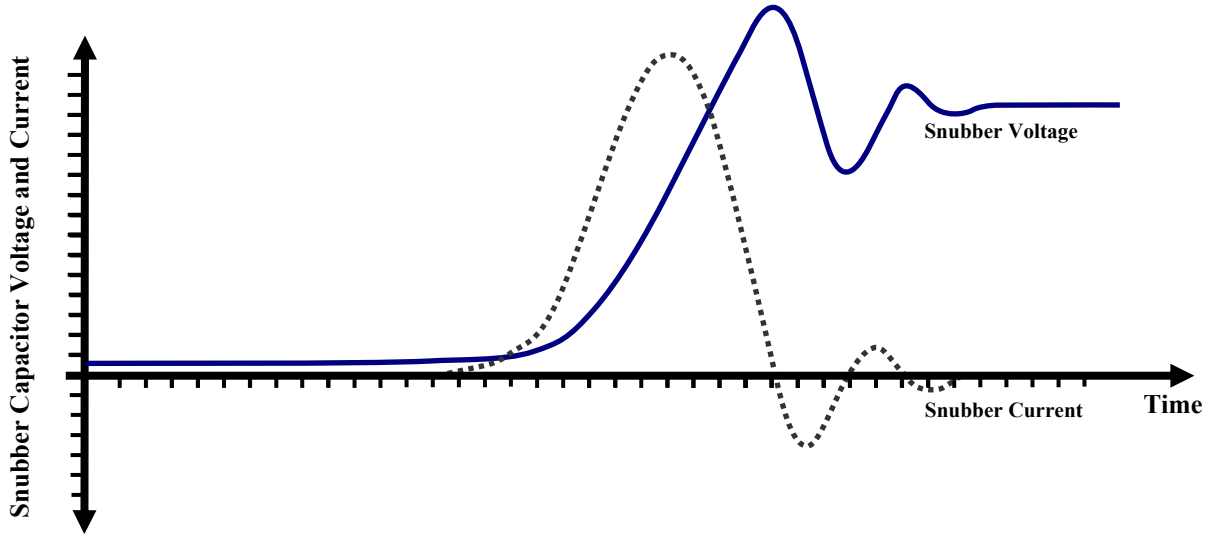


Figure 6: Expected Snubber Waveform[11]

The voltage spike that occurs at the end of the turn-off waveform (V_{DM}) is voltage overshoot that results from the anode voltage being under-damped. One way that this voltage spike can be reduced is by increasing the size of the snubber capacitor to dampen out the rise in anode voltage. The major drawback to increasing the amount of snubber capacitance is the increase in the voltage rise time (time it takes for the anode voltage to rise to its final value) and an overall increase in switching power losses.[13]

Safe operation of a GTO thyristor depends in large part on successfully maintaining proper voltage bias across the gate-cathode junction. The gate-cathode junction has to be forward biased (higher voltage at the gate relative to the cathode) in order to inject current into the gate and drive the device into its conduction state. Likewise the gate-cathode junction needs to be reverse biased in order to remove current from the gate terminal and force the GTO thyristor into its voltage blocking state. A GTO thyristor will fail if the gate-cathode junction does not remain reverse biased during the entire turn-off transition.[14]

1.3 Research Objective

Gate Turn Off thyristors potentially have a higher current turn-off capability when used in pulsed power applications than when used for standard power electronics applications (e.g. motor drives, power converters, etc…). Researchers at the IAT-UT used a GTO thyristor to interrupt between 2 and 2.5 times its rated capacity for current turn-off in an inductive pulse forming network.[15] Researchers at the Propulsion Physics Laboratory (PPL) at the Soreq Nuclear Research Center in Israel constructed a XRAM pulse generator that used GTO thyristors to interrupt 175% of their rated capacity for current turn-off.[16] (XRAM generators use a set of inductors connected together with switches to allow the inductors to charge up in series and then discharge in parallel.) Both of these experiments utilized GTO thyristors in pulsed power application where the switches were used to interrupt large current levels at very low pulse repetition rates (switching frequencies <1Hz).

Most power electronic switches are designed and built for use in industrial applications such as motor drives, power supplies, converters, inverters, etc. These applications typically use switching frequencies in the kilohertz range (>1kHz) in order to achieve waveform fidelity without excessive filtering. Since there is little commercial demand for high current pulse power systems, most power electronic switches are simply not designed for or tested at very low switching frequencies, like those encountered in a railgun pulse power source. As such, the actual turn-off capability of GTO thyristors at low switching frequencies might be significantly higher than their nominal rated current interruption capability. (The rated current interruption capability is given by the manufacture based on the use of the device in standard commercial applications.)

The current interruption capability of the GTO thyristors might also be increased because of the circuit topology of the pulsed power applications in which they are used. In the inductive pulse forming network developed at IAT-UT (shown in Figure 1 and described in Appendix A), the capacitor connected across the two storage inductors absorbs the spike in inductor voltage that occurs when the GTO thyristor opens to interrupt the charging current. This reduces the overall stress on the GTO thyristor during turn off and may in part be responsible for the increase in its current interruption capability.

The goal of this project was to investigate two mechanisms that had the potential to influence the current interruption capacity of a GTO thyristor in an inductive turn-off switching system. The research project was divided into two components: (1) Designing and fabricating the test circuit that was used to explore the inductive turn-off switching performance of the GTO thyristors. (2) Using the test circuit to investigate GTO thyristor switching characteristics in order to systematically determine which circuit and control factors influence the current interruption capacity of GTO thyristors.

The investigation of the GTO thyristors examined the effect of one control factor and one circuit factor on the current interruption capability of the GTO thyristors. The research effort examined how the snubber circuit (specifically the amount of snubber capacitance) affected the current interruption capability of the GTO thyristors. Additionally, the research project examined how the magnitude of the turn-off gate current pulse affected the current interruption capability of the GTO thyristors. Ultimately, this project determined a method for increasing the current interruption capability of GTO thyristors.

2 TEST CIRCUIT DESIGN

The first part of this project involved designing and constructing the testing apparatus to examine the switching characteristics of a GTO thyristor. The test circuit was designed to use a GTO thyristor to interrupt increasing amounts of current in an inductive pulse forming network; the point at which the GTO thyristor failed to turn-off represented the maximum current interruption capacity of the GTO thyristor for the particular gate current pulse magnitude and snubber circuitry. The project tested a series of identical Motorola MGTO-1000 thyristors with different gate current pulse magnitudes and varying snubber capacitances and measured the maximum current interruption capacity for each setup.

The research effort used a test apparatus to generate the current pulses which were interrupted by the GTO thyristors. The test circuit consisted of an inductive pulse former, a gate drive circuit, and a control circuit. The inductive pulse former consisted of a simple inductor and freewheeling diode and was used to generate and shape the current pulses that were interrupted by the GTO thyristors as shown in Figure 7. The gate driver circuit generated the gate current pulses that were required to turn the GTO thyristors on and off. The control circuit operated the gate driver circuit and determined the timing delay and pulse widths of the current pulses generated by the gate driver circuit. The following sections detail the design of each element of the apparatus and the overall implementation and construction of the test apparatus.

2.1 Inductive Pulse Forming Circuit

The primary element of the test circuit was the inductive pulse former used to generate the current pulses that were interrupted by the GTO thyristors. The actual inductive pulse forming circuit was very simple; as shown in Figure 7 it consisted of a bank of capacitors connected in series with the GTO thyristor and an inductor. The diode in parallel with inductor provided a path for the inductor current when the GTO turned off. Additionally, the pulse forming circuit incorporated a snubber circuit to protect the GTO thyristor during device turn off.

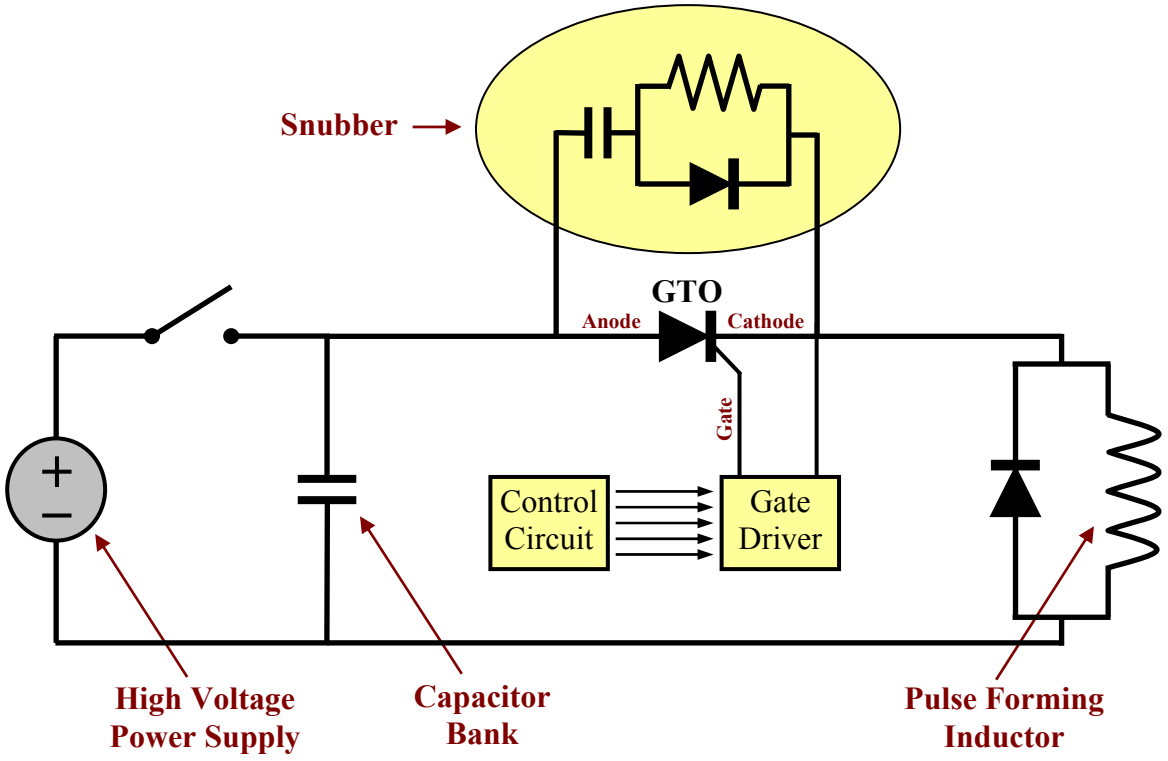


Figure 7: Inductive Pulse Forming Circuit Concept

The inductive pulse former behaved like a series RLC (resistor, inductor, and capacitor) circuit. Initially, the high-voltage power supply would charge the capacitor bank to some prescribed voltage level. When the GTO thyristor was turned on, the capacitor bank would discharge through the inductor and generate a quasi-sinusoidal current pulse through the GTO thyristor. The duration of the pulse was determined by the relative sizes of the inductor and capacitor while the peak amplitude of the current pulse was determined by the initial voltage on the capacitor bank and the overall resistance of the circuit.

The circuit uses a capacitor bank rather than a battery to supply the inductor charging current in order to limit the amount of energy that was released when the GTO thyristor failed. The project consisted of a series of experiments in which sets of identical GTO thyristors were tested using specific levels of gate current to turn the devices off and using a specific sized capacitor in the snubber circuit. Each GTO thyristor was used to interrupt progressively higher current levels until the device failed to turn off. If the circuit had used a battery bank instead of a capacitor bank, the battery bank would have uncontrollably discharged into the circuit each time

one of the GTO thyristors failed. The capacitor bank used in the test circuit was comprised of four 2400uF electrolytic capacitors (Cornel Dubilier DCMC242T450) connected in parallel. The capacitors have a maximum voltage rating of 450V and an equivalent series resistance (ESR) of 54.7mΩ (refer to the datasheets in Appendix C for additional capacitor specifications). The capacitors were chosen for the test circuit because they were available from a previous railgun project.

The particular semiconductor device that was selected for this project was the Motorola MGTO-1000 thyristor; this particular thyristor was selected because it afforded the best tradeoff between switch cost and current blocking capability. The MGTO-1000 thyristors were obtained for $150 per switch; while larger GTO thyristors, such as the ABB 5SGA 06D4502, cost over $1000 per switch. The MGTO-1000 thyristors have a maximum current interruption capability of 70A and a 1000V voltage blocking rating. In comparison, the 5SGA 06D4502 GTOs had a 600A maximum interruptible current rating and a 4500V voltage blocking rating. (Refer to the datasheets in Appendix C for additional specifications on the MGTO-1000 thyristor.)

The inductive pulse forming circuit was simulated using a SPICE-based circuit simulation program called Micro-Cap© to determine the appropriate size of the pulse forming inductor. Since the amount of capacitance was fixed by the number and size of available capacitors, the inductance value was adjusted to achieve the desired rise time for the anode current in the GTO thyristor. The rise time needed to be short enough to keep the current pulse within the rated fusing parameter of the MGTO-1000 thyristor while still being representative of a railgun application. Fusing is a physical device parameter that describes how a device handles high current levels and is found by multiplying the length of the current pulse (in seconds) by the square of root-mean-square (rms) anode current (in Amperes). The resistance of the inductor dominates the overall resistance of the circuit and was chosen to limit the maximum possible anode current. (The initial charge voltage of the capacitor bank determined the peak anode current for a given experiment; but that value could not exceed the maximum anode current set by the inductor resistance.) In addition to a fusing parameter, the GTO thyristors had a maximum possible surge current that could not be exceeded. The MGTO-1000 thyristors had a $167A^2s$ fusing rating and a 200A surge current rating.

A nominal resistance of 1Ω was chosen for the inductor to limit the maximum possible anode current (generated when the capacitor bank is charged to its maximum voltage of 450V) to 250A, which is 125% of the rated surge current of the MGTO-1000 thyristor. With the capacitance and resistance of the pulse forming circuit fixed, the current rise time of the pulse forming circuit was measured with a computer simulation for various inductor values. A target inductance of 5mH was chosen for the pulse forming inductor to provide a nominal 8ms current rise time (time to peak current). Figure 8 shows the anode current that was generated in the GTO thyristor for various initial voltages on the capacitor bank. The inductance and resistance values provide for a maximum fusing that is 140% higher than the rated fusing of the MGTO thyristor as shown in Equation 1. (Since the current pulse is quasi-sinusoidal, computing the rms value based on the peak current is reasonable.) For the inductive turn-off circuit, the maximum possible anode current and circuit fusing are both greater than the MGTO-1000's rated values in order to account for possible safety margins in the device specifications. Since a goal of the project was to test the failure point of the GTO thyristors, the inductive pulse forming circuit was designed to ensure that the GTOs could be driven to failure regardless of those safety margins.

$$Irms \approx \frac{Ipeak}{\sqrt{2}} \approx \frac{250A}{\sqrt{2}} \approx 176.8Arms$$
$$f \approx Irms^2 t \approx (176.8A)^2(0.008s) \approx 250A^2s$$

Equation 1: Maximum Fusing of the MGTO Thyristor

2.2 Simulation Validation of the Inductive Pulse Forming Circuit

The inductive pulse forming circuit was constructed using an air-core wire-wound inductor to shape the current pulses. The inductor was designed specifically for this project (refer to Section 2.7) using 16AWG magnet wire and a 4.5 inch diameter core. The inductor had a nominal DC inductance of 4.62mH and a nominal resistance of 1.03Ω. The inductance value set the nominal rise time of the GTO thyristor anode circuit to approximately 7.5ms. (Rise time is defined as the time from when the GTO thyristor first turns on to the time when the anode current reaches its peak value.) The plot shown in Figure 8 illustrates the rise time of the anode current pulses and shows that the peak anode current was a determined by the initial voltage on the capacitor bank. The graph was generated using the Micro-Cap© program to simulate the pulse forming circuit with various capacitor bank charge voltages.

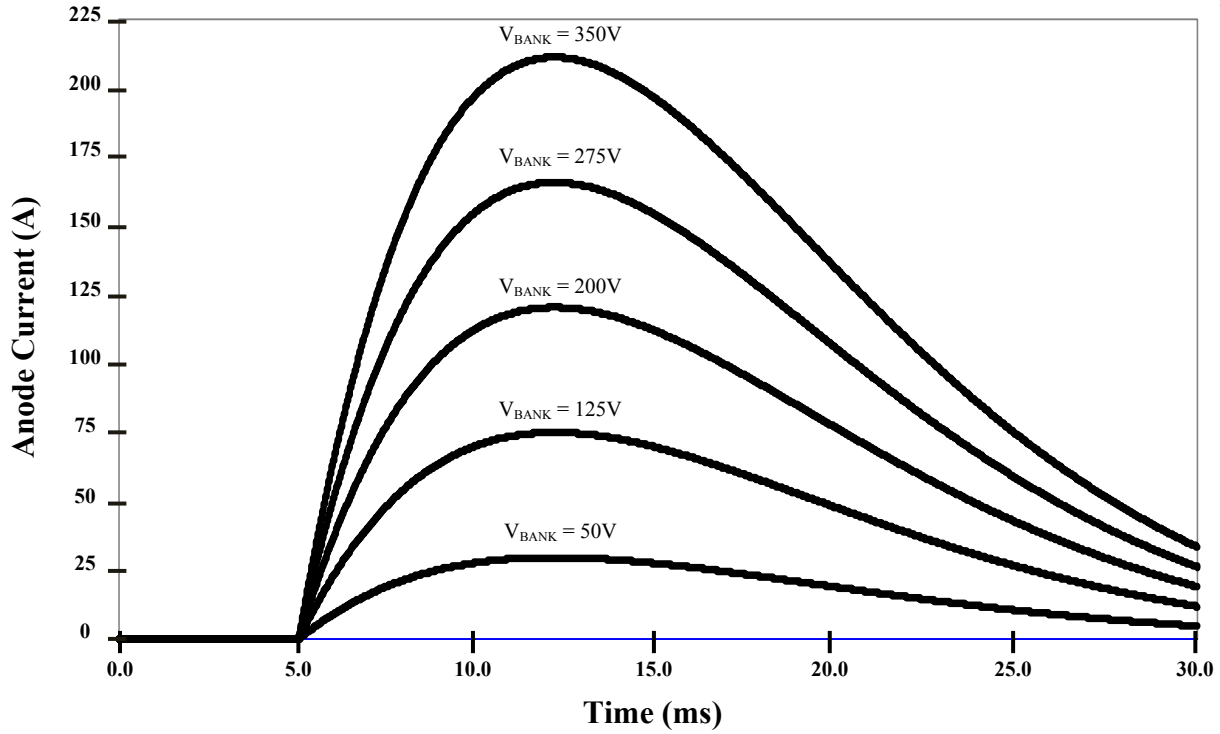


Figure 8: Anode Current as Function of Capacitor Bank Voltage

As shown in Figure 7, the inductive pulse forming circuit incorporates a snubber (refer to Section 1.2) to protect the GTO thyristor from excessive voltage rise during turn-off switching. The Micro-Cap© simulation of the inductive pulse forming circuit was used to determine appropriate values for the snubber resistance and capacitance. The capacitor needed to be large enough to limit the rate of anode voltage rise but not so large as to prevent the GTO thyristors from being turned off. The snubber resistor needed to be large enough to prevent excessive current when the snubber capacitor discharged following turn-on of the GTOs but not so large as to prevent the snubber capacitor from discharging completely.

The graphs in Figure 9 were generated using a Micro-Cap© simulation of the test circuit and show how the snubber circuit behaved each time the GTO thyristor was cycled (switched on and then switched off). The top plot shows the voltage on the snubber capacitance, the middle plot shows the current in the snubber resistor, and the bottom plot shows the current in the snubber diode. The plots illustrate how the snubber capacitor discharges through the resistor when the GTO turns on (at 2ms in the graphs) and then charges through the diode when the GTO turns off (at 8ms in the graphs).

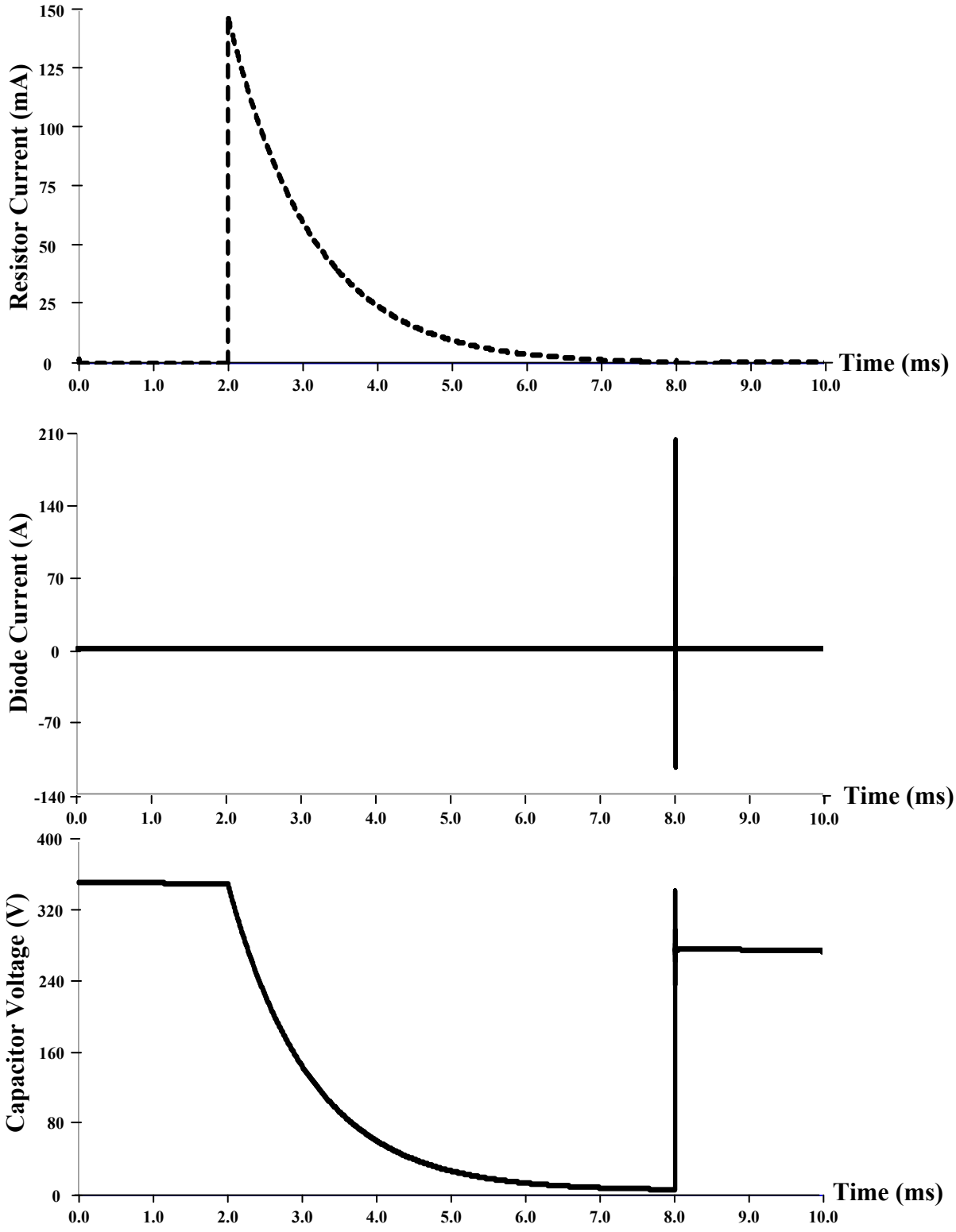


Figure 9: Snubber Variables During GTO Thyristor Turn On and Turn Off

The values of the snubber resistance and capacitance were selected to ensure that the turn-off voltage spike did not exceed the GTO thyristor's rated blocking voltage (1kV) and that the snubber capacitor would completely discharge within 4ms of GTO thyristor turn on. In comparison, the pulse forming inductor was sized to provide a total time to peak anode current of 7.5ms. An additional factor that went into selecting the capacitor was the availability of high voltage capacitors with low equivalent series resistance (ESR) and low equivalent series inductance (ESL). The selected snubber capacitor was a 470nF double metalized polypropylene capacitor (Vishay MGMM 2222-383-30474) that had a voltage rating of 1kV, a typical ESR less than 6mΩ, and a typical ESL less than 23nH. The selected snubber resistor was a 1kΩ 2-Watt non-inductive resistor and the snubber diode was a fast recovery power diode (Fairchild RURG8060) with a 600V blocking capability and a 200A surge conduction capability (refer to Appendix C for additional specifications on these components).

The importance of using a snubber circuit to protect the GTO thyristors during turn off is illustrated in Figure 10. The figure was generated using a Micro-Cap© simulation of the pulse forming test circuit, where the GTO was modeled using a resistor/transistor model developed at Drexel University.[17] The solid line shows the anode voltage across the GTO and the dotted line shows the anode current through the GTO. When the GTO thyristor turns off, the anode voltage always overshoots its steady-state value due to the stray inductance in the circuitry (a 50nF inductor was used in the simulation for the stray inductance). Without a snubber capacitor to dampen the rate of voltage rise, the peak anode voltage overshoot can exceed the voltage capacity of the GTO. (The GTO thyristor used in the simulation had a blocking voltage of 1kV.)

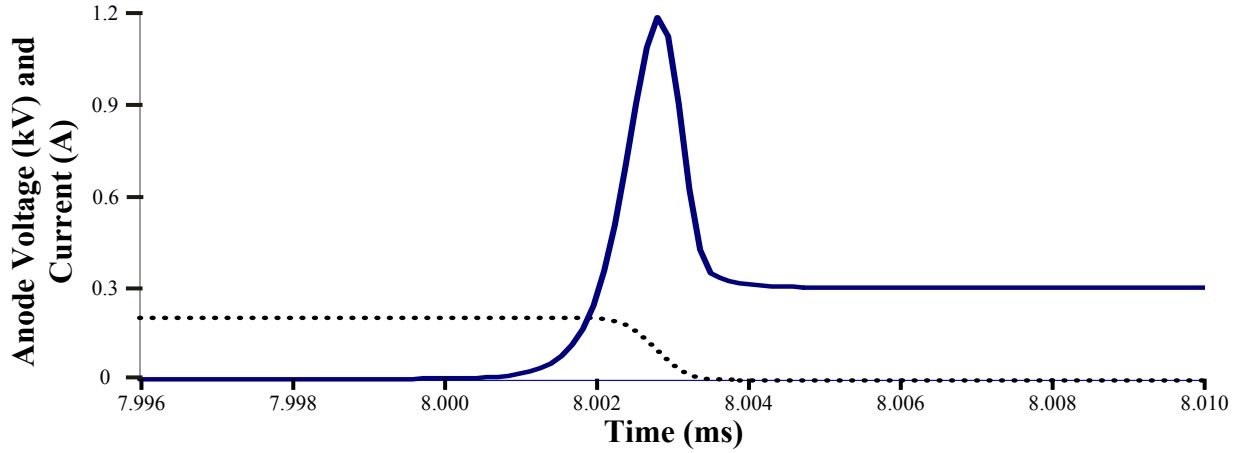


Figure 10: GTO Turn Off without an RC Snubber

The simulated turn-off characteristics of a snubbered GTO thyristor are shown below in Figure 11; the figure was generated using the same Micro-Cap© simulation and GTO Thyristor model used to generate Figure 10. The solid line represents the anode voltage across the GTO while the dotted line represents the current through the GTO. The anode voltage still overshoots its final value, but the magnitude of the overshoot is significantly reduced by the snubber circuit. Notice that the simulated switching characteristics shown in the graph are very similar to the expected turn-off characteristics of a GTO thyristor shown in Figure 5.

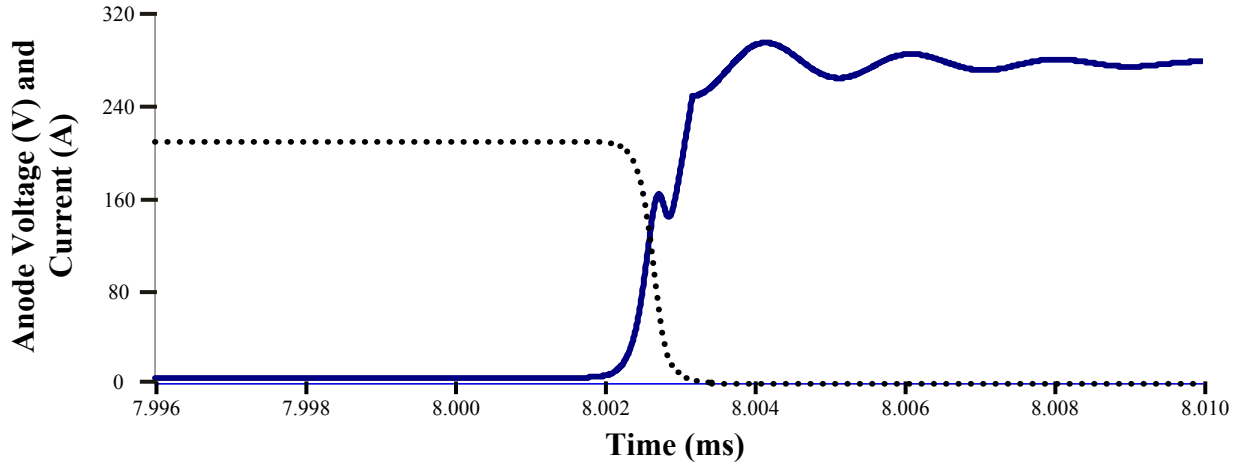


Figure 11: GTO Turn Off with an RC Snubber

2.3 Gate Drive Circuit

Gate Turn Off thyristors are current-controlled devices that are turned on and off by injecting current into or removing current from their gate terminal (refer to Section 1.2). A GTO thyristor is turned on by forward biasing the gate-cathode junction to generate a positive current into the gate. To turn off the GTO thyristor, the gate-cathode junction is reversed biased in order to generate a negative current out of the gate terminal.

For this project, a gate drive circuit was designed and constructed to generate the current pulses required to turn the GTO thyristor on and off. The gate drive circuit, shown in Figure 12, is a two phase-leg H-bridge that was implemented using four power Metal Oxide Silicon Field Effect Transistor (MOSFET) switches.[18] Prior to turning the GTO thyristor on or off, the isolated power supplies (Von and Voff) pre-charged the capacitors C1 and C2; the power supplies were then disconnected from the circuit via switches S1 and S2. The gate drive circuit generated the

turn-on and turn-off current pulses by switching on opposing pairs of MOSFETs. The turn-on pulse was generated by switching on M1 and M3 to connect the gate terminal to the positive voltage +Von (across C1) and the cathode terminal to H-bridge common rail; this would forward bias the gate-cathode junction and allowed current to flow into the gate and out of the cathode. The turn-off pulse was produced by switching on M4 and M2 to connect the cathode terminal to positive voltage +Voff (across C2) and the gate terminal to the H-bridge common rail; this would reverse bias the gate-cathode junction and allowed current to flow into the cathode and out of the gate. The resistors Ron and Roff ensure that the gate current does not exceed the maximum gate current rating of the GTO thyristor.

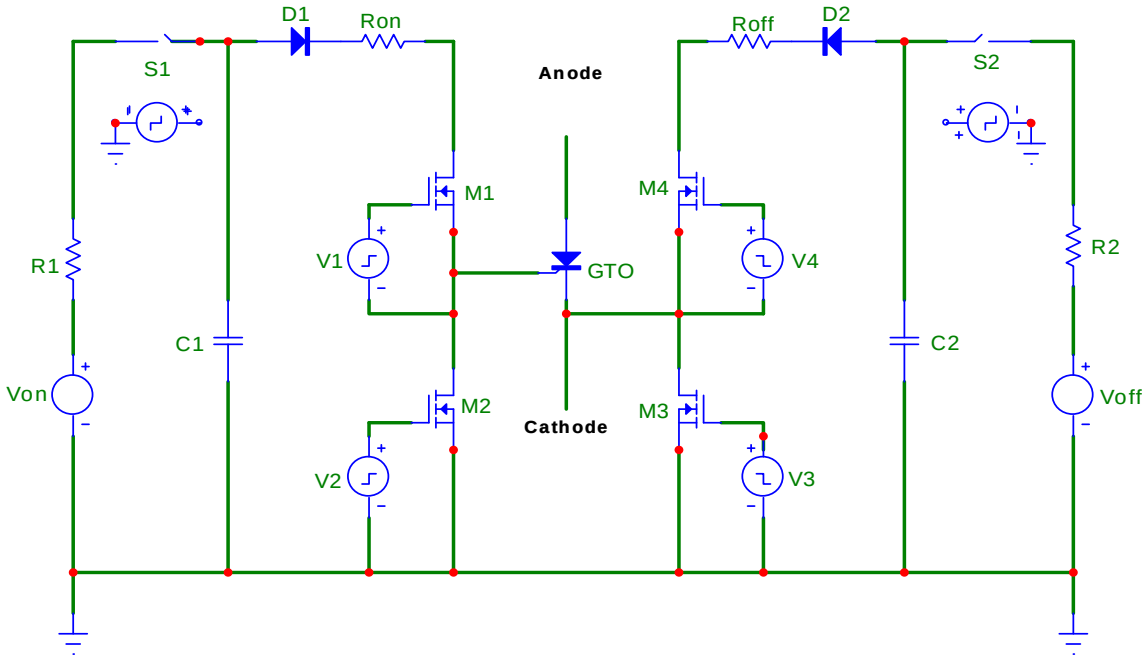


Figure 12: MOSFET H-Bridge Gate Drive Circuit

Every GTO thyristor requires some minimum amount of turn-on current to switch from the voltage blocking state to the current conduction state. The minimum turn-on current value is typically specified in a device datasheet and represents the minimum current required to drive the npn transistor region into saturation and turn on the GTO thyristor; for the MGTO-1000 thyristor, the minimum turn-on current was 300mA. In a similar manner, there is a minimum turn-off current required to switch a GTO thyristor from the current conduction state to the voltage blocking state. This value changes depending upon the amount of current being interrupted by the GTO thyristor; typically the minimum turn-off current value is 20% - 30% of

the anode to cathode current.[19] Past research shows that larger gate current pulses improve the switching characteristics of GTO thyristors. Increasing the magnitude of the turn-on current pulse allows the GTO thyristor to turn on faster and decreases the turn-on power losses. Likewise, increasing the size of the turn-off current pulse forces the GTO thyristor to turn-off faster and can reduce the amount of turn-off stress placed on the GTO thyristor.[20] Unfortunately, the past research has only considered higher-frequency industrial power switching applications like electric motor drives.

The gate drive circuit was designed to provide a variety of different turn-on and turn-off current pulses. The timing of the MOSFETs was controlled by an external logic circuit (refer to Section 2.5) and could be adjusted to change the pulse width of the turn-on and turn-off current pulses. The magnitude of the turn-on and turn-off current pulses was determined by the charging voltage applied to the gate drive capacitor banks (C1 and C2 in Figure 12). Both charging voltages were supplied by external power supplies and could be changed independently. In the inductive test circuit, the GTO thyristor was located between the high voltage side of the capacitor bank and the pulse forming inductor. Because the cathode of the GTO thyristor was not connected directly to the ground of the test circuit, the gate drive circuit could not have the same ground connection as the inductive test circuit. Consequently, the gate drive circuit used isolated power supplies to charge up the two capacitor banks.

The external logic circuit that was used to control the overall timing of the gate driver circuit could not source enough current to directly drive the MOSFET switches. (The logic circuit incorporated Transistor Transistor Logic (TTL) components and was limited to ~25mA of current per control output.) Consequently, the control circuit employed a Fairchild Semiconductor HIP4082 driver chip to control the individual MOSFET switches. The driver chip had four outputs to control the H-bridge MOSFETs and could source at least 1.0A of current per output (refer to the datasheets in Appendix C for additional specifications on the HIP4082 gate driver chip). The outputs of the H-bridge driver chip were connected to the MOSFETs using small power resistors. The driver chip was controlled using five TTL logic signals that were generated by an external logic circuit (see Section 2.5 for further detail on the external logic circuit).

2.4 Simulation Validation of the Gate Drive Circuit

Unfortunately, there were no convenient simulation models of GTO thyristors suitable for modeling the exact turn-on and turn-off characteristics of the gate-cathode junction. As a result, it was not possible to simulate the exact behavior of the gate drive circuit. In order to explore the general behavior of the gate drive circuit, the gate-cathode junction was modeled with a resistor and capacitor (a 500mΩ resistor modeled the junction resistance while a 500uF capacitor modeled the storage charge that had to be supplied to the gate-cathode junction during turn off).

Using the simplified gate-cathode model, the gate drive circuit was simulated to ensure that the turn-on and turn-off current pulses would be large enough to control the GTO thyristor properly. Figure 13 shows the simulated current in the gate-cathode junction and illustrates the general behavior of the gate drive circuit. For this particular simulation, the initial voltage on the turn-on capacitor bank (C1 in Figure 12) was 5V while the initial voltage on the turn-off capacitor bank (C2 in Figure 12) was 15V.

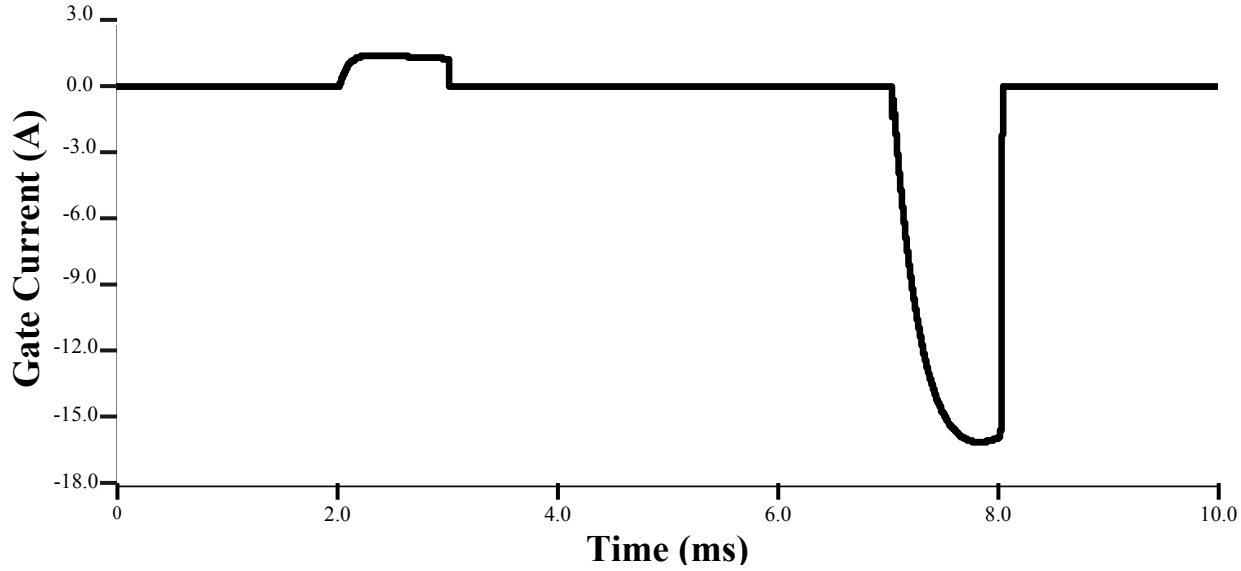


Figure 13: Gate Control Current (I_{GATE})

Because the exact characteristics of the gate-cathode junction were not known, the gate driver circuit was constructed (refer to Section 3.1 for a discussion of the physical layout of the gate drive circuit) so that the capacitance and charge voltage of the turn-on and turn-off capacitor banks could be adjusted to achieve successful operation of the GTO thyristors.

2.5 External Control Circuit

The gate drive circuit consisted of four power MOSFET semiconductor switches connected in an H-bridge configuration. The MOSFETs were turned on and off using an H-bridge driver chip that was controlled by an external logic circuit (refer to Section 3.1 for details on the bridge driver). An external logic circuit, implemented on an Altera DE2 Development and Education Board, was used to control when the MOSFETs were turned on and for how long. The DE2 board, shown in Figure 14, is a commercially available Field Programmable Gate Array (FPGA) that can be programmed for various computer and digital electronic applications.

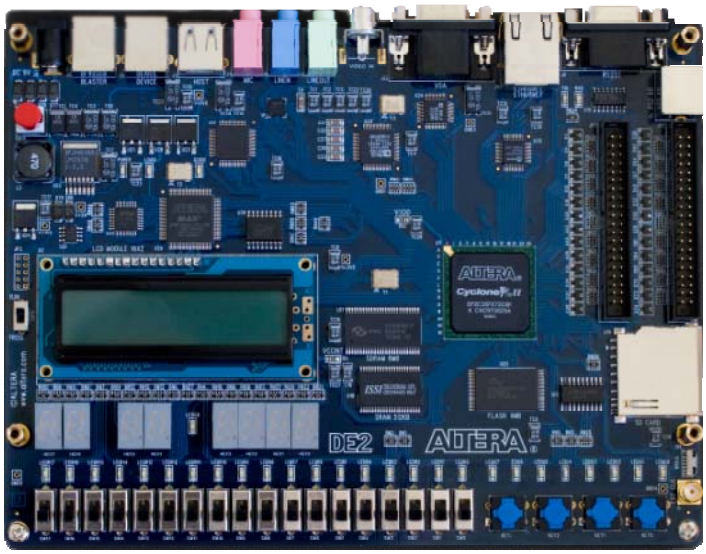


Figure 14: Altera DE2 Development Board

The switch control logic was programmed into the DE2 board using a hardware description language called VHDL. (The program code developed for this experiment is included in Appendix B of this report.) The logic circuit functioned according to the diagram shown in Figure 15. There were four separate timing values that had to be input into the DE2 board: the delay time until the start of the turn-on pulse, the pulse width of the turn-on pulse, the delay time until the start of the turn-off pulse, and the pulse width of the turn-off pulse. Once the timing values were input, the logic circuit waited until the experiment was initiated before generating the logic signals that controlled the H-bridge driver chip. The logic circuit was designed to check the timing values to ensure that the turn-on pulse and turn-off pulse did not overlap. If the timing values were invalid, then the logic circuit would not allow the experiment to be initiated.

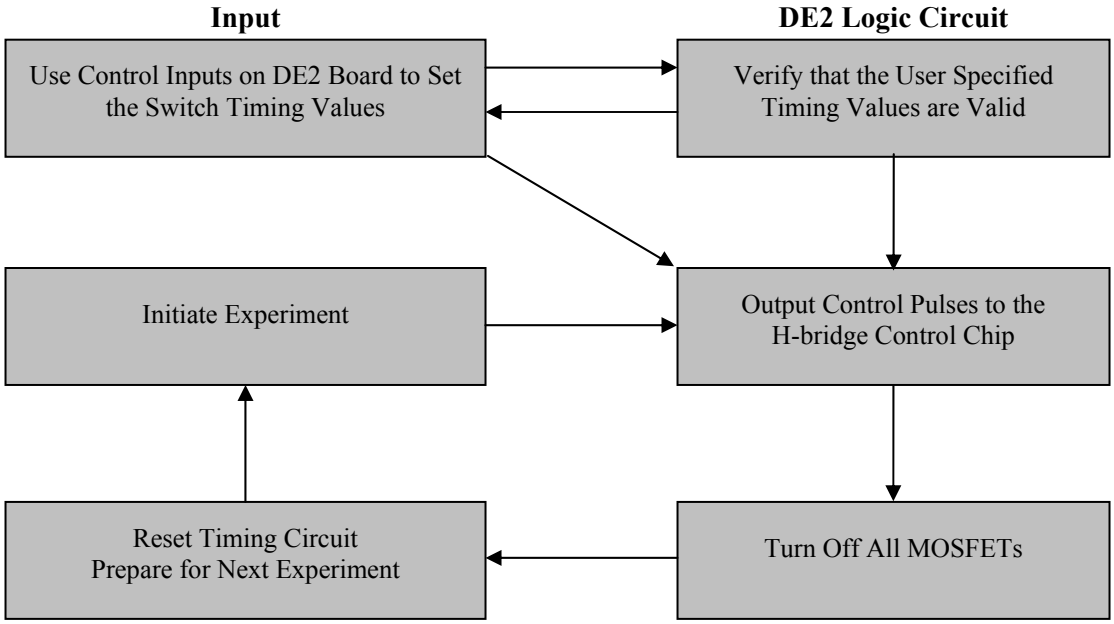


Figure 15: Flow Chart of Control Logic Program

2.6 Validation of the External Control Circuit

The operation of the logic circuit was tested by running timing simulations of the VHDL code used to set up the logic circuit on the Altera DE2 Development and Education Board. These timing simulations were performed using a VHDL development program called Quartus II. For each simulation, the program generated a set of waveforms similar to those shown in Figure 16 to indicate the output signals of the DE2 logic board.

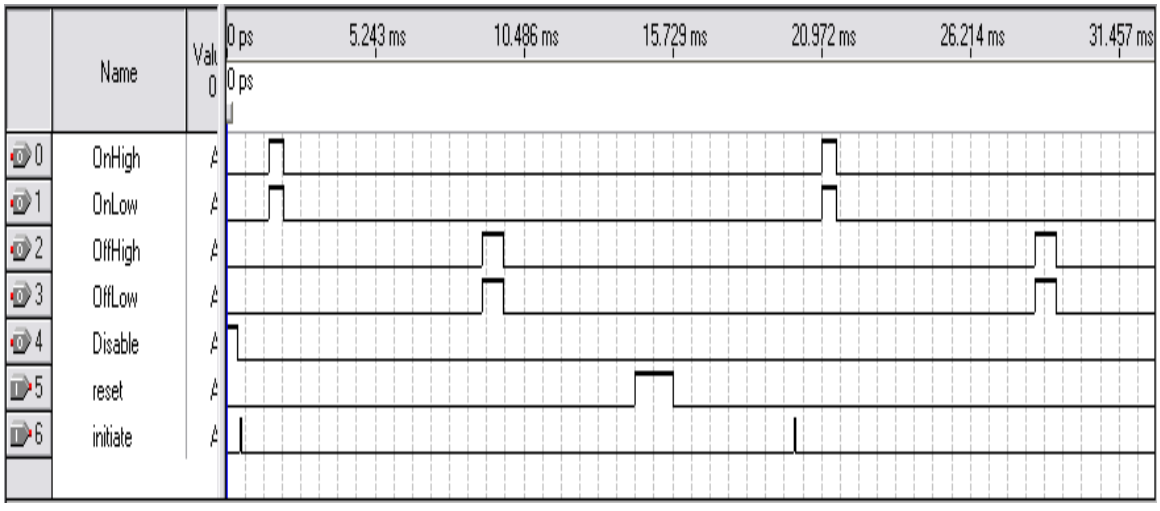


Figure 16: Timing Simulation of the H-Bridge Driver Logic Circuit

The simulation waveform shown in Figure 16 was generated using a turn-on delay of 1.5ms, a turn-on pulse width of 500us, a turn-off delay of 9ms, and a turn-off pulse width of 750us. The logic circuit produced five signals to control the H-bridge driver chip; the signal labeled OnHigh controlled the MOSFET labeled M1 in Figure 12, the signal OnLow controlled the MOSFET M3, the signal OffHigh controlled the MOSFET M4, and the signal Offlow controlled the MOSFET M2. The fifth control signal was a master disable that would turn off all four MOSFETs regardless of the other inputs.

The timing simulation illustrates the flowchart process shown in Figure 15. After the switch timing values were input into the logic circuit, the logic circuit would wait until the experiment was initiated (the momentary spike in the input "initiate") before it would output the MOSFET control signals. Once the experiment was initiated, the program would output the control signals with the appropriate timing (notice that the MOSFETs are turned on in pairs: M1-M3 and M2-M4). Following completion of the experiment, the program would wait to receive a reset signal before allowing another run of the experiment.

2.7 Pulse Forming Inductor

As described previously, the inductive test circuit for the GTO thyristor used an inductor to shape the anode current pulse. During the design of the test circuit, it was determined that the pulse forming inductor should have 5mH of inductance and a DC resistance of 1Ω (see Section 2.1). The required inductance of the pulse former was fairly high, so the inductor had to be custom made for the project. The pulse forming inductor was designed as an air-core wire-wound inductor in order to simplify the fabrication process. (An air-core wire-wound inductor is fabricated by wrapping magnet wire around a non-ferrous core.)

The pulse forming inductor was designed such that it could be fabricated using standard diameter PVC pipe and standard gauge magnet wire. Tightly wrapping magnet wire around a PVC pipe creates an air-core solenoid that has an inductance that can be roughly approximated using the Wheeler formula shown in Equation 2; where r is the average radius of the coil, l is the length of the coil, n is the number of wire wraps (turns), and L is the inductance of the coil. (Average radius is used to account for multiple wire layers.)

$$L=\frac{r^2n^2}{9r+10l}$$

Equation 2: Wheeler Approximation for Single-Layer Air-Core Solenoid

The resistance of the pulse forming inductor depended on the length and size of wire used to fabricate the inductor and is described by Equation 3. In the equation, *r* is the average radius of the coil, *n* is the number of wire wraps, and ρ is the resistivity of the wire (related to wire size and material)

$$R=2\pi rn\rho$$

Equation 3: Resistance of Pulse Forming Inductor

Equation 2 and 3 were used to determine the coil length *l* and number of wire wraps *n* needed to achieve the target inductance and resistance using a standard diameter of PVC pipe and a readily available gauge of magnet wire. Ultimately, it was decided to fabricate a four layer air-core solenoid using 16 gauge magnet wire (ρ = 1.557mΩ/ft) and a 4-inch diameter PVC pipe (the pipe had an outer diameter of 4.5”). The selected PVC pipe gave the inductor coil a diameter of 4.5-inches and required a coil length of *l* = 2.715 inches and *n* = 209 wire turns to achieve the desired 5mH of inductance. (Section 3.3 describes the assembly of the pulse forming inductor.)

3 TEST CIRCUIT FABRICATION

In order to simplify the fabrication of the composite GTO thyristor test circuit and minimize stray inductance in the circuit connections, a printed circuit board (PCB) was developed to integrate the inductive pulse former, the gate drive circuit, and the control interface circuitry. The PCB allowed the various circuit components to be quickly and easily connected together and ensured proper electrical connection between the various components. For example, the MGTO thyristors were soldered onto the circuit board using small connection pins while the large 2400uF capacitors were screwed onto the circuit board with large threaded terminals.

3.1 Printed Circuit Board

The printed circuit board was fabricated using a commercially-available circuit board printing service from a company called ExpressPCB (www.expresspcb.com). The company provides a free circuit board development program to generate the design files necessary to have a circuit board printed. This program was used to develop a printed circuit board that integrated all of the components needed to test the switching of the GTO thyristor.

The first step in the process of developing the circuit board was to generate a single circuit schematic that integrated the various components of the composite test circuit; the circuit schematic was then used to develop the physical layout of the components. Figure 17 shows the schematic diagram that integrated the various components required to test the switching performance of the GTO thyristor; the GTO thyristor (labeled S1) is located near the center of the schematic.

The gate drive circuit consisted of four MOSFET switches (Q1–Q4), sixteen capacitors (C10–C25), two resistors (R26 and R27), two diodes (D6 and D7), and two BNC connectors (BNC2 and BNC3). The inductive pulse forming circuit consisted of the four high voltage capacitors (C1–C4), two diodes (D1 and D2), the pulse forming inductor L, the snubber circuit (C5, R5, and D5), the MGTO device (SW1), and a BNC connector (BNC1). The various components connected to the high voltage capacitors (R12–R25, C6 and C7, and S2) allowed the capacitors to be rapidly (less than two seconds) discharged by pressing the pushbutton SW. Closing the pushbutton turned on an SCR thyristor (S2) and discharged the capacitor banks through a set of six 25W high power resistors (Ohmite – 825F20RE).

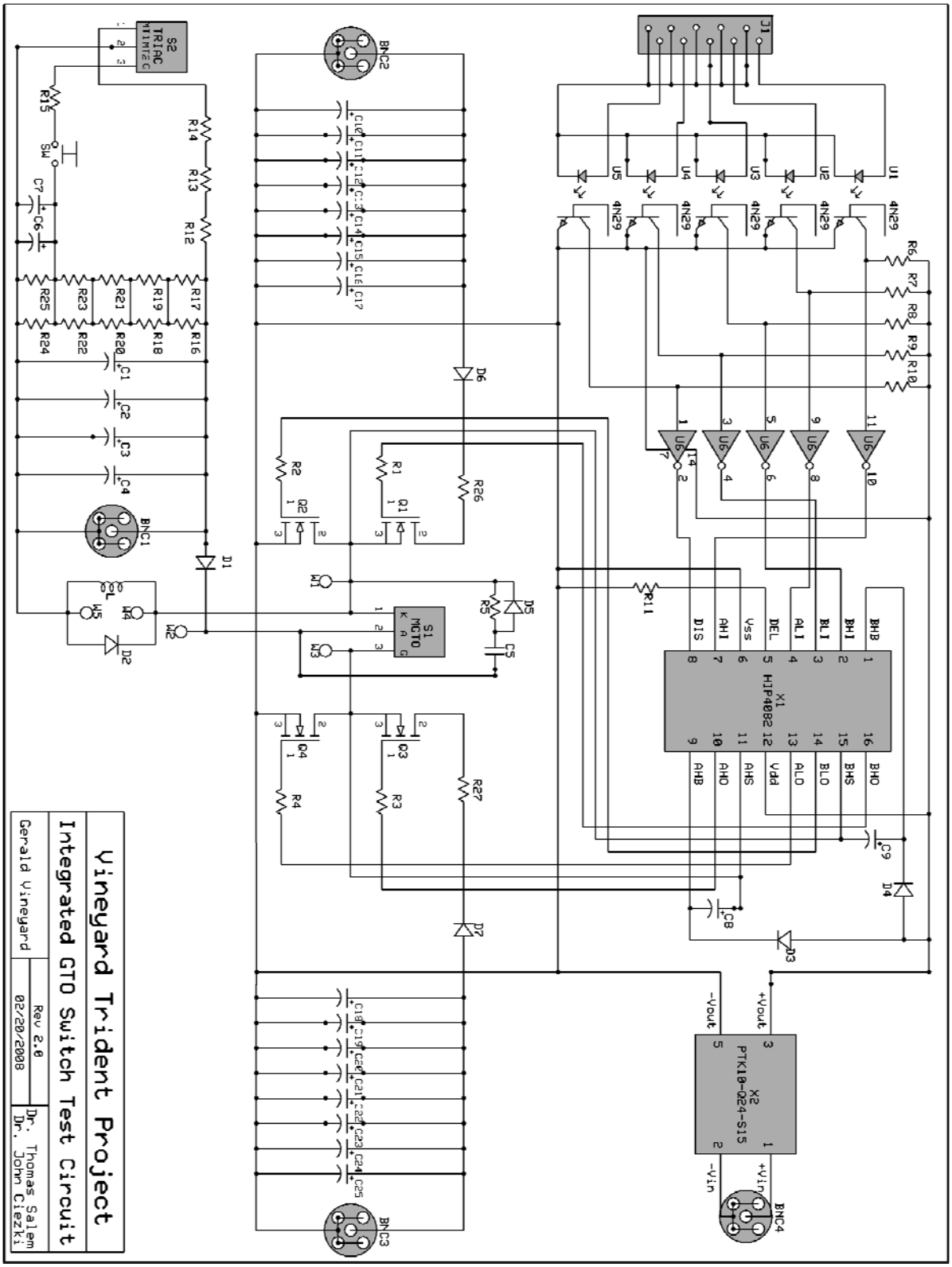


Figure 17: Circuit Schematic – GTO Test Circuit

All of the components in the top half of the circuit schematic were part of the gate drive circuit and the control logic interface. As discussed in Section 2.3, the gate drive circuit was an H-bridge composed of four MOSFET switches (Q1-Q4) that were operated by an H-bridge driver chip (X1). The MOSFETs chosen for the gate driver were fast switching power MOSFETs (International Rectifier - IRF1010Z) rated to conduct 75A of source-drain current. Because the MOSFETs required 12-15V of gate-source voltage in order to turn on, the circuit used a special H-Bridge FET Driver (Intersil – HIP4082) chip to control the four MOSFETs. The H-Bridge driver had five control inputs that allowed the external logic circuit to control the timing of the MOSFET switches.

The cathode of the GTO thyristor was not connected directly to the ground plane of the test circuit (negative terminal of the high voltage capacitors); consequently, the entire gate drive circuit had to be electrically isolated from the rest of the circuit. The power for the H-Bridge driver was supplied using a 15V isolated DC-DC converter (V-infinity – PTK10-Q24-S15). The two gate driver capacitor banks (C10-C18 and C19-C25) were charged using isolated DC power supplies that were connected to the circuit board via BNC connectors (BNC2 and BNC3). Even the control signals from the external logic circuit (supplied through the junction J1 in Figure 17) were isolated from the gate driver circuit using a series of Photodarlington Optocouplers (Fairchild – 4N30). Because the optocouplers (U1 through U5) invert the control signals from external logic source, the outputs from the optocouplers were connected to the H-bridge driver through a CMOS hex-inverter (U6).

Once all the required components of the composite test circuit were integrated into a single circuit schematic, the ExpressPCB™ program was used to develop the physical layout of the composite circuit board. The final layout for the board is indicated in the image shown in Figure 18. The yellow lines and text indicate the location and identification of the various components of the test circuit and were printed onto the actual circuit board as the silkscreen layer. The red areas show where copper traces and regions were printed onto the top surface of the circuit board, while the green areas represent copper traces and regions that were printed onto the bottom surface of the board. Note: The top copper layer was made transparent for display purposes so the areas that are brownish-orange had copper printed on both sides of the board.

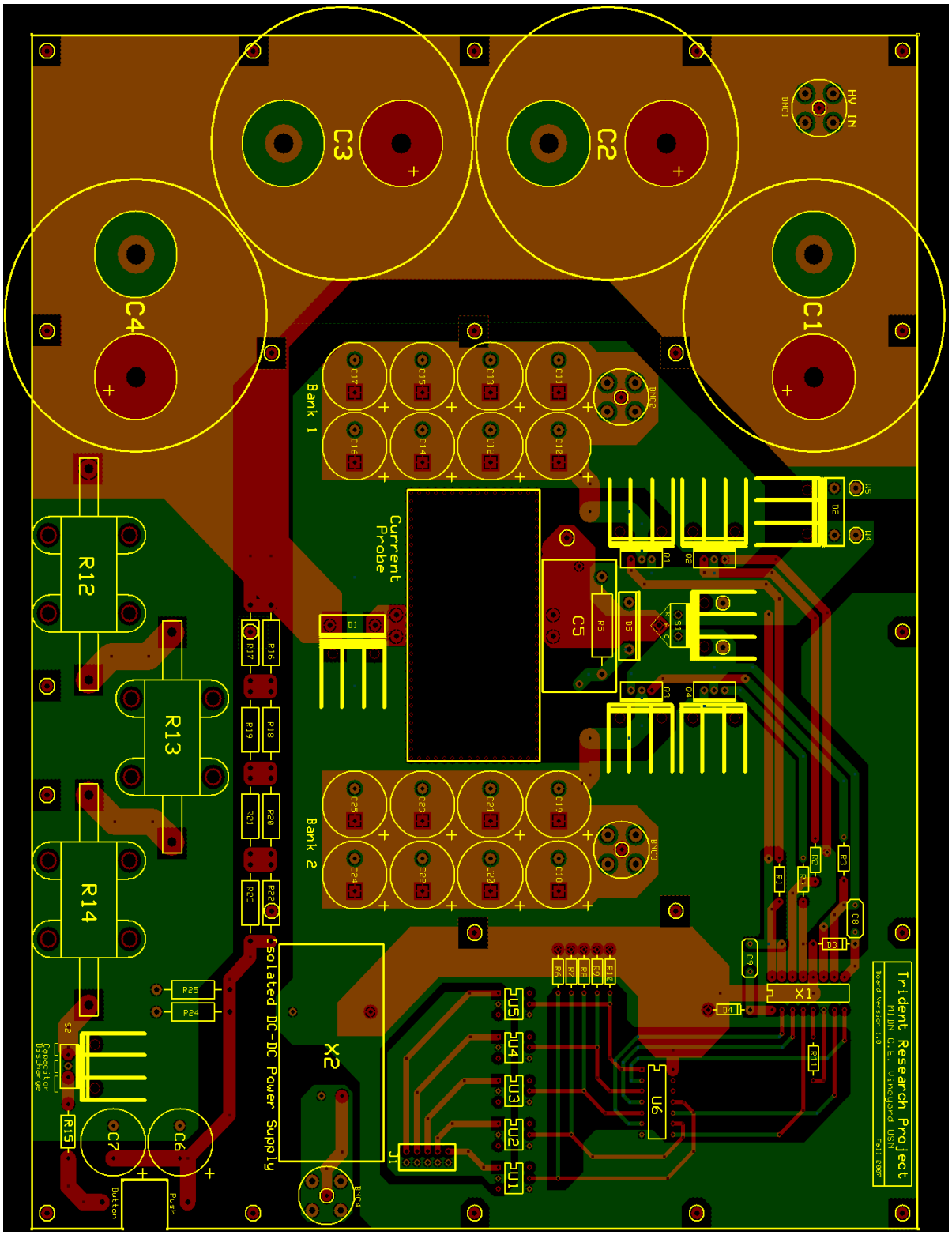


Figure 18: Physical PCB Layout – Composite Test Circuit

The most important factor that was considered during the development of the board layout was minimizing stray circuit inductances. Stray inductance (L_s) is generated by current loops in a circuit that enclose large surface areas; stray inductance is harmful to circuits because it can cause harmful voltage spikes ($L_s {}^{dI}/_{dt}$) across switches and other components with rapidly changing currents. In order to minimize stray inductance, critical circuit components had to be placed as close to each other as possible.

For this project, the circuit board was laid out so that the four MOSFETs of the gate drive circuit were as close to the GTO thyristor as possible. The GTO thyristor and the MOSFETs required heatsinks, which limited how close the components could be placed together. (The heatsinks are represented as large "finned" objects shown next to the MOSFETs, the MGTO switch, and the diodes in Figure 18) The gate drive capacitor banks were located as close as possible to the GTO thyristor and a large ground plane (green layer) was placed under the capacitor banks to reduce the effective loop areas of the gate current paths as much as possible. Finally, the circuit traces from the H-bridge FET driver to the MOSFETs were placed as close to each other as possible to minimize the loop area of each MOSFET control path. The MOSFETs were connected to the H-bridge driver chip with two circuit traces each; one of the traces connected to the gate of the MOSFET while the other connected to the source of the MOSFET and provided a return path for the control signal.

Another important factor that was considered during the development of the board layout was experiment instrumentation and data collection. The goal of the research project was to fully characterize the switching behavior of a GTO thyristor in an inductive pulse forming network. To characterize the GTO thyristors, the currents and voltages at the anode and the gate of the GTO thyristor had to be measured. The circuit board was laid out as best as possible to make these measurements more convenient. Each terminal of the GTO thyristor was connected to a solder point that allowed for convenient attachment of differential voltage probes. A large area was laid out on the board to allow placement of two Rogowski current transducers (Power Electronic Measurements CWT Ultra Mini, Model 1) to measure the currents at the anode and gate of the GTO devices. The Rogowski coils were special current probes that could be attached around the gate and anode terminals of the GTO thyristor and were selected to minimize stray inductance in the circuit.

Finally, the layout of the capacitor bank discharge circuit (shown in the upper right corner of Figure 17 and the lower left corner of Figure 18) was designed to provide maximum safety when operating the pushbutton. The pushbutton trigger was physically located as far as possible from the high voltage areas of the circuit board. The capacitors discharged through six 25W 20Ω power resistors that were connected together to provide 30Ω of total resistance. (The resistors were place at the locations marked R12, R13, and R14 in Figure 18.) Since the maximum possible capacitor voltage was 450V, the power resistors ensured that the discharge current never exceeded the 15A current conduction capacity of the discharge switch; the discharge switch was a TRIAC (Littlefuse – Q6015L5) rated to block 600Vand conduct 15A. (For this circuit, the TRIAC operated like an SCR thyristor)

3.2 High Voltage Power Supply Controller

The high voltage capacitor bank was charged using an external high voltage power supply that was connected to the circuit board with a BNC connector (BNC1). This project used a 350W MATSUSADA power supply that could deliver 500V at 700mA. The power supply was left over from a previous railgun research project and did not come with any sort of control interface. (Most MATSUSADA laboratory power supplies have built in control circuitry or come with commercially manufactured control interfaces.)

In order to use the power supply as the power supply for the high-voltage capacitor bank, a control interface had to be implemented. As shown in Figure 19, the control interface circuit consisted of two 100k potentiometers, two toggle switches, and two BNC connectors.

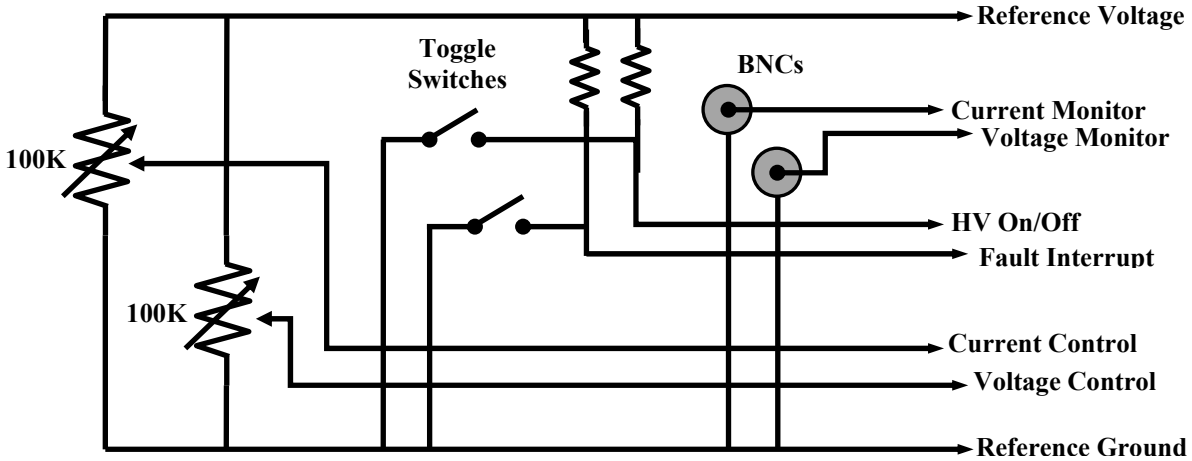


Figure 19: High Voltage Power Supply Interface Circuit

The interface was connected to the power supply via a custom fabricated 8-pin cable. Four of the pins supplied input signals to the interface circuit, while the other four pins carried the control signals back to the power supply. The inputs consisted of a 10.25V DC reference signal, a reference ground, a voltage monitoring input and a current monitoring input. The outputs consisted of two logic signals (0V or 10V), the current control signal, and the voltage control signal. The current and voltage control signals ranged from 0-10V and were generated by the two 100K potentiometers. The two control signals determined what percentage of the power supply' maximum voltage and current capability was output. (For example, a 5V voltage control signal set the output voltage to 50% of the power supply's 500V maximum output voltage. Similarly, a 7.5V current control signal limited the output current to 75% of the power supply's 700mA maximum output current.)

The two toggle switches generated active low logic signals to enable the power supply's high voltage output. In order for the power supply to generate an output voltage, both switches had to be closed to set the HV On/Off and Fault Interrupt control signals to 0V. The HV On/Off switch was opened just prior to each test of the GTO thyristors to shut off the HV power supply; following each switch test, the HV On/Off switch was closed to turn the power supply back on and charge up the high voltage capacitor bank. (The power supply was turned before each test to prevent excessive current discharge in the event that the GTO failed.) The Fault Interrupt switch acted as a master "kill switch" that would trip the power supply's internal breaker in the event of a major fault in the test circuit. Whenever the Fault Interrupt switch was opened, the power supply had to be completely reset before its high voltage output could be re-enabled.

The voltage and current monitor inputs to the interface circuit provided feedback as to the current and voltage output of the high voltage power supply. Just like the current and voltage control outputs, the two monitor inputs varied from 0-10V and represented 0-100% of the power supplies maximum voltage and current output capability. The BNC connectors allowed the current and voltage monitor inputs to be measured with a laboratory multimeter.

The interface circuit was constructed in a 3"x5"x1" plastic project box and was used to adjust the charge voltage on the high-voltage capacitor bank to achieve the desired peak anode current. The control box also included an LED display (not shown in Figure 19) that activated whenever the high voltage output was enabled.

3.3 Pulse-Forming Inductor

The test circuit used an air-core wire-wound inductor to shape the anode current pulses that were interrupted by the GTO thyristors (see the discussion in Section 2.7). The simulations of the inductive turn-off circuit showed that the pulse forming inductor should have 5mH of inductance and a nominal resistance of 1Ω. Based upon these values, it was decided to implement the pulse forming inductor by fabricating a four-layer air-core solenoid using 4-inch diameter PVC pipe and 16 gauge magnet wire. The inside diameter of the inductor coil (same as the outside diameter of the pipe) was D = 4.5 inches, the required coil length was l = 2.715 inches and the required number of wraps was n = 209 turns.

The inductor was constructed using a lathe to hold the PVC pipe such that the magnet wire could be wrapped tightly around the inductor. In order to simplify the fabrication process, the inductor was designed assuming that the wire turns would be laid down without any spacing between adjacent turns. Each layer was wrapped with a special high-dielectric tape, known as Kapton™ tape, to prevent any unforeseen voltage transients from generating electric arcs between the layers of the inductor. Figure 20 shows the cross section of the inductor.

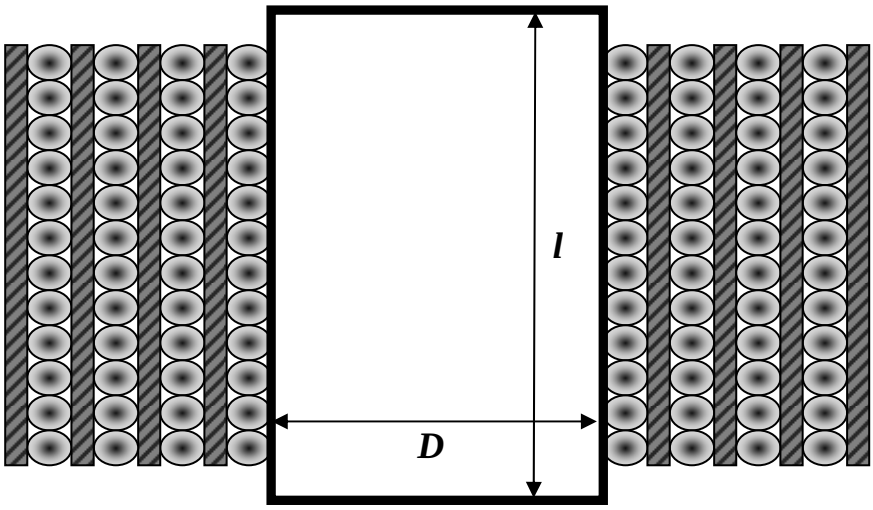


Figure 20: Four-Layer Air-Core Inductor

Following fabrication, the inductance of the air-core wire-wound inductor was measured using an inductance-capacitance (LC) meter. The inductor had an approximate inductance of 4.62mH, which was ~8% smaller than the target inductance of 5mH. The inductor had a DC resistance of 1.03Ω, which was almost identical to the desired resistance of 1 Ω.

3.4 GTO Thyristor Test Circuit

Following their design and fabrication, the individual components of the test circuit were assembled on the printed circuit board. The circuit board provided a rigid platform on which to mount the circuit component and ensured proper electrical contact between the various circuit components. Additionally, the printed circuit board guaranteed easy access to the terminals of the GTO thyristor to simplify measurement of the voltage and current at the anode and cathode of the GTO.

The assembled test circuit is shown below in Figure 21. The gold colored components at the bottom of the circuit are the high power resistors that were used to rapidly discharge the high-voltage capacitor banks (the other three resistors are on the underside of the board and are not shown in the picture). The MGTO thyristor is located in the center-back of the picture just in front of its heatsink. The four MOSFETs are located to the left and right of the GTO and are mounted on heatsinks. The inductor is the large white object in the very back of the picture. The high-voltage capacitors and the capacitors for the gate drive circuit were mounted on the underside of the board and are not visible in this picture. (The screw terminals for the high-voltage capacitors can be seen on the left edge of the picture and the gate drive capacitor banks are labeled.)

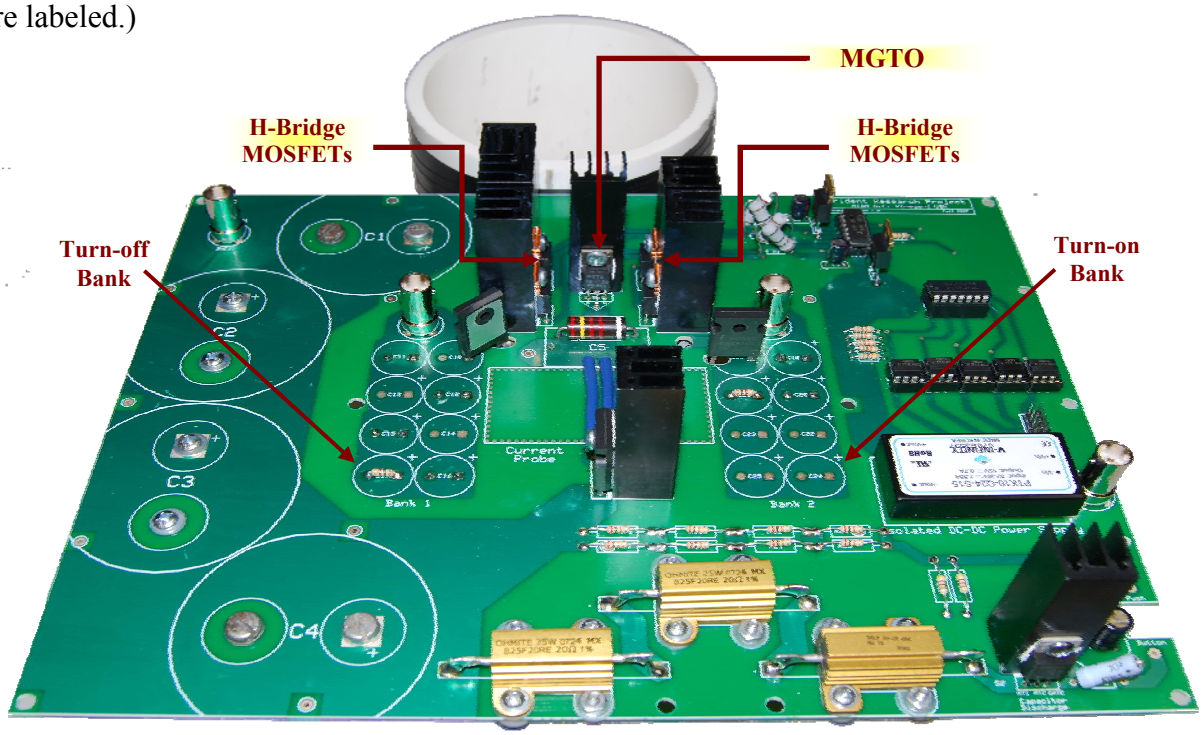


Figure 21: GTO Thyristor Test Circuit

4 TEST CIRCUIT VALIDATION

Before investigating the current interruption capacity of the GTO thyristors, a significant amount of research effort was spent verifying that the test circuit was operating as designed. During this part of the project, the operation of the capacitor bank dump circuit, gate driver circuit, external logic circuit, and instruments were investigated. Several modifications to the gate drive circuit were necessary to make the test circuit function properly. Additionally, the instrumentation scheme was modified to better capture the turn-off characteristics of the GTO thyristors.

4.1 Capacitor Bank Discharge Circuit

By far the most straightforward part of the test circuit to verify was the capacitor dump circuit. The capacitor bank was charged up to 200V and the TRIAC (S2 in Figure 17) was triggered. An oscilloscope with a differential probe was used to record the capacitor bank voltage as the capacitors discharged. The voltage waveform, shown below in Figure 22, indicates that the dump circuit has an RC time constant $\tau \approx 300$ms. This time constant is consistent with the expected RC time constant of 288ms (30Ω multiplied by 9.6mF).

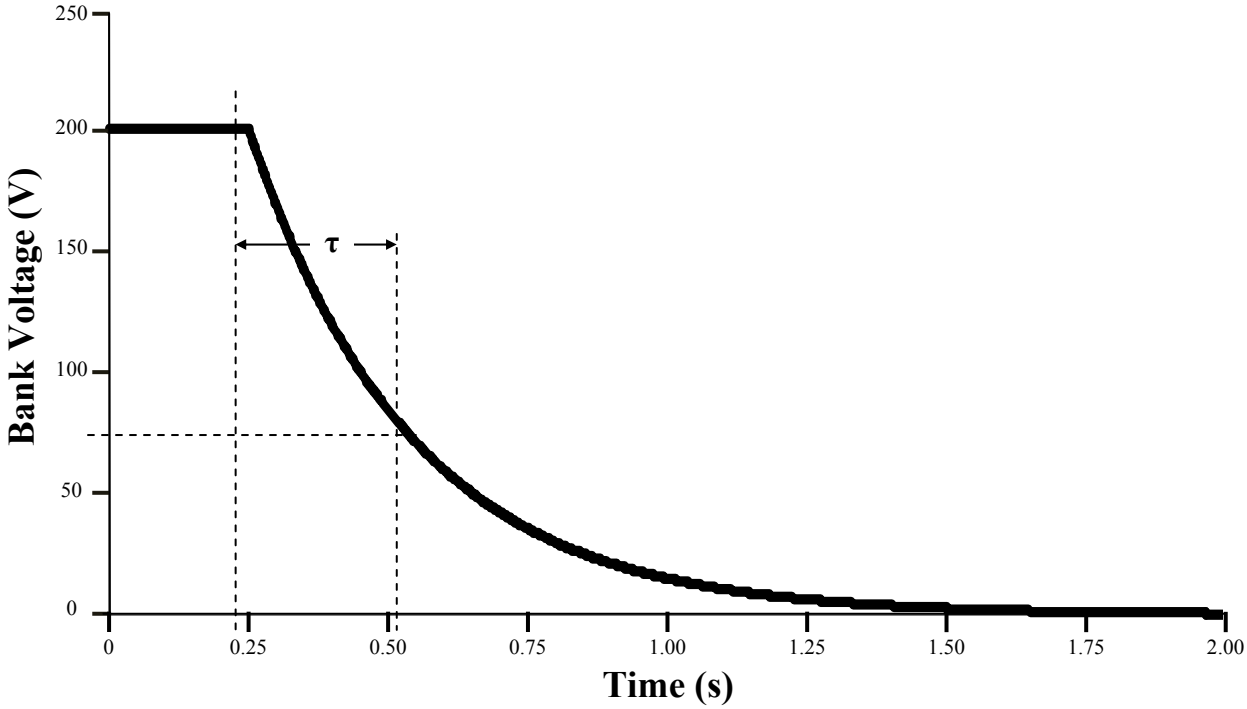


Figure 22: Capacitor Bank Discharge Waveform

4.2 H-Bridge Driver Chip and External Logic Circuit

The operation of the external logic circuit was tested in conjunction with the H-bridge MOSFETS, H-bridge driver chip, and the control input isolation circuitry. A 1kΩ resistor was soldered onto the printed circuit board in place of the gate and cathode terminals of the MGTO thyristor to provide a circuit path for the turn-on and turn-off legs of the H-bridge gate driver. The voltage across the test resistor was positive if the MOSFETs in the turn-on leg of the H-bridge were on and negative if the MOSFETs in the turn-off leg of the H-bridge were on. If both sets of MOSFETs were off, the voltage across the test resistor was zero. An oscilloscope was used to capture the test resistor voltage waveforms to verify the operation of the H-bridge and the associated driver circuitry.

The oscilloscope generated a series of voltage waveforms that showed the behavior of the gate drive circuit for a variety of pulse timing values. Figure 23 shows the voltage waveform that was generated by the H-bridge circuit with a 1ms turn-on delay (D_{on}), a 6m turn-off delay (D_{off}), and 1ms pulse widths for the turn on and turn off pulses (t_{on} and t_{off}). The four timing values were varied to determine the minimum timing values that the logic circuit and H-bridge driver chip could support. The tests determined that the minimum possible pulse width was 1ms for both the turn-on and turn-off pulses and the minimum time between pulses was 500ns; these minimums were set by the physical characteristics of the H-bridge driver chip.

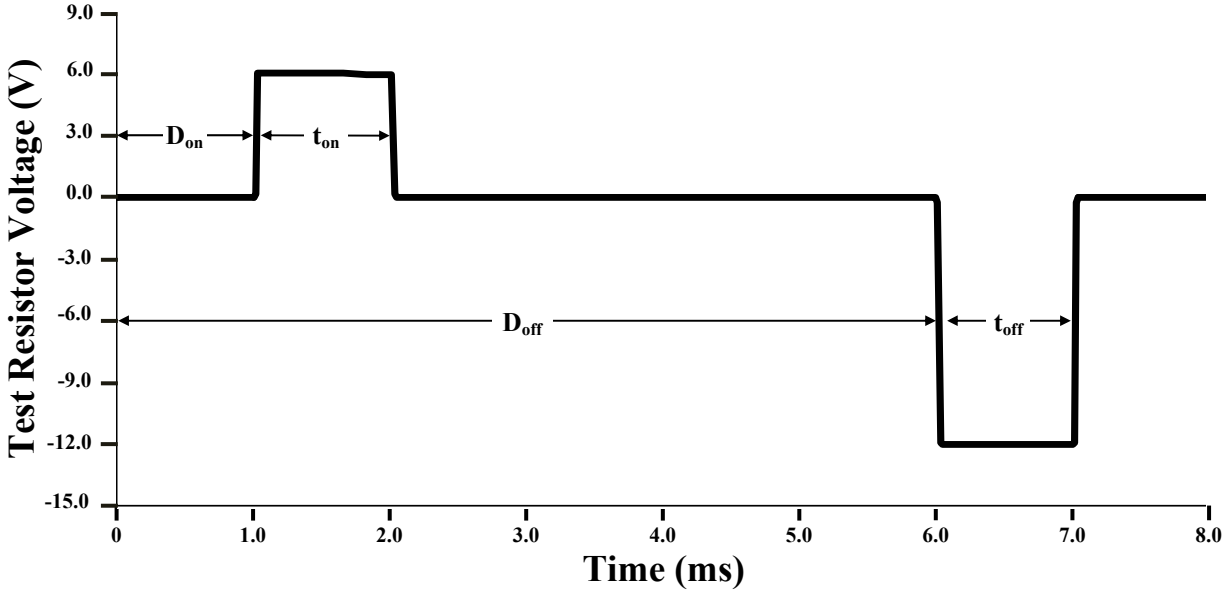


Figure 23: H-bridge Driver Verification Waveform

4.3 Gate Drive Circuit

Following verification of the H-bridge driver, the test resistor was replaced with an MGTO thyristor and the circuit was tested to verify that the gate driver was capable of turning the GTO thyristor on and off. The initial tests of the GTO thyristors demonstrated two unforeseen problems with the design of the gate drive circuit and led to several post assembly modifications to the printed circuit board and gate driver circuit. Once those modifications were made, the gate driver and test circuits operated as originally intended.

The first few tests with the GTO thyristors showed that the peak magnitude of the turn-on current pulse was in excess of 300A even when the gate voltage during turn-on was only 500mV. The excessive current caused the turn-on pulse to exceed the peak power dissipation of the gate junction and resulted in several failed GTO thyristors. (The datasheet gives 10W as the maximum turn-on gate power for the MGTO-1000 thyristor.) This particular problem was solved by inserting a small value (~2.5Ω – 3W) resistor between the turn-on capacitor bank and the high-side MOSFET of the H-bridge turn-on leg. (This resistor is represented as R27 in the circuit schematic shown in Figure 17.)

The initial tests also showed that the current through the gate-cathode junction of the GTO thyristor was not behaving as expected. The tests showed that the gate current would pulse positive (the gate current was referenced with positive current flow going into the gate terminal) and then continue flowing after the turn-on MOSFETs in the H-bridge shut off. As a result of the unexpected current characteristics, the gate-cathode junction would not always remain negatively biased when the GTO thyristors were turned off (refer to the discussion in Section 1.2), which would cause the GTOs to fail.

After several switch failures, the problem was solved by adding diodes between the gate driver capacitor banks and the high-side H-bridge MOSFETs. The diodes (D6 and D7 in the circuit schematic shown in Figure 17) ensured that the gate current only flowed when the MOSFETs were turned on and ensured that the gate current flowed from the high-side MOSFET to the low-side MOSFET of whichever H-bridge leg was in use. With the two diodes in place, the gate driver generated the proper gate current waveforms as shown in Figure 24. The plot in Figure 24 shows a positive current pulse at 2.5ms which correspond to the gate current pulse used to turn on the GTO and a negative current pulse at 7.0ms which was used to turn off the

GTO. The turn-on and turn-off current pulses had dramatically different characteristics; the turn-on pulses were significantly wider than the turn-off current pulses and the minimum required turn-on current was significantly smaller than the minimum current needed to turn off the GTOs.

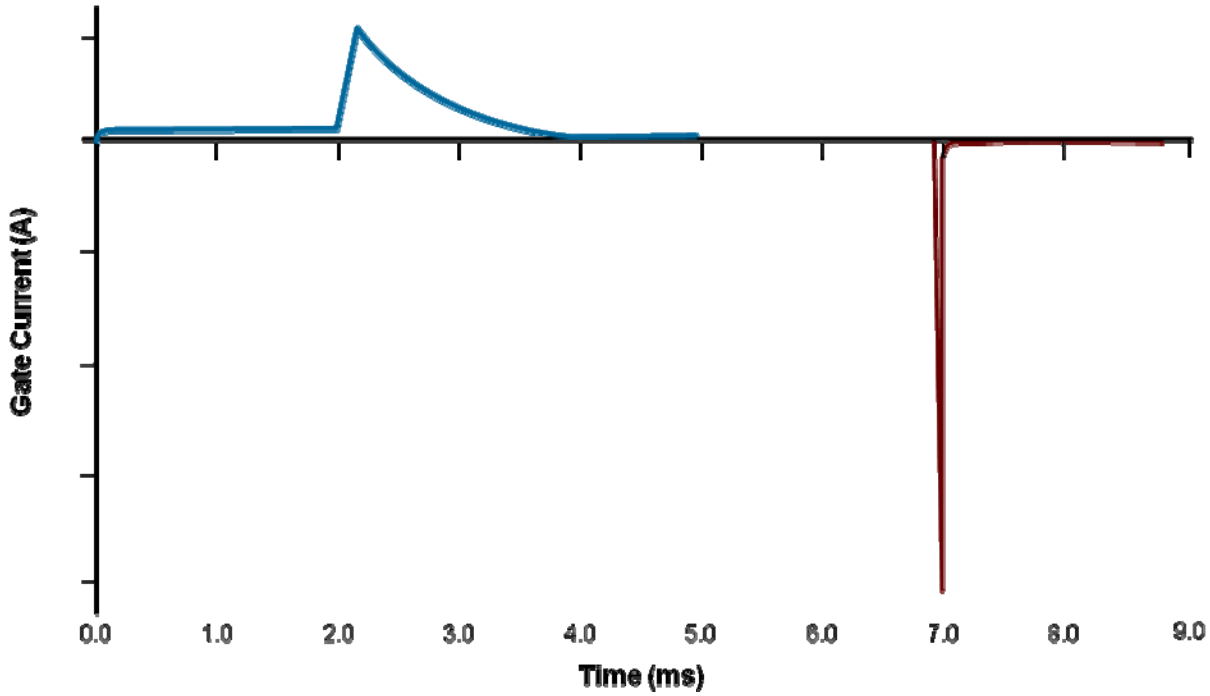


Figure 24: Gate Current Characteristic of the Modified Gate Drive Circuit

The turn-on and turn-off current pulses had different characteristics because the PN semiconductor junction (see Figure 2) between the gate and cathode of the GTO behaved very differently depending on the applied voltage bias. When the turn-on pulse was applied, the PN junction was forward biased and behaved very much like a forward biased diode. Consequently, the turn-on current pulse looked like a capacitor (the turn-on capacitor bank) discharging through a resistor (the forward biased PN junction). When the GTO turned off, the PN junction transitioned from forward biased to reverse biased and caused the gate-cathode to behave like a diode in reverse recovery. When a diode turns off, its current goes negative for a short period to remove the excess charge carriers from the device; this process is known as reverse recovery. In the case of the GTO thyristor, the turn-off current pulse forced the PN junction into reverse recovery and removed the charge carriers from the gate-cathode junction. The width of the turn-off current pulse was determined by the amount of time needed to remove the charge carriers from the gate-cathode junction and was largely a function of the peak turn-off current.

4.4 Instrumentation (Rogowski Coils)

The final step in the circuit validation process was to check the instrumentation to ensure that the voltages and currents in the test circuit were being measured properly. The test circuit was designed such that the voltage and current at both the gate and anode of the GTO thyristor could be measured and recorded with an oscilloscope. The voltages were measured using calibrated differential voltage probes (Tektronix P5200) that were connected into the circuit via clip on leads; the reference point for both the anode and gate voltages was the cathode of the GTO thyristor. The currents were measured using Rogowski current transducers (Power Electronic Measurements CWT Ultra Mini, Model 1) placed around the gate and anode leads of the GTO thyristor.

Proper use of the Rogowski coils was verified by using one of the Rogowsk coils to measure the anode current in the GTO thyristor over a range of capacitor bank voltages. The measurements were compared with the expected peak current determined using a Micro-Cap© simulation of the test circuit. Figure 25 contains a plot of simulated peak current (blue squares) and measured peak current (red diamonds) as functions of the capacitor bank voltage. From the plot it can be seen that the current measurements closely matched the expected current values.

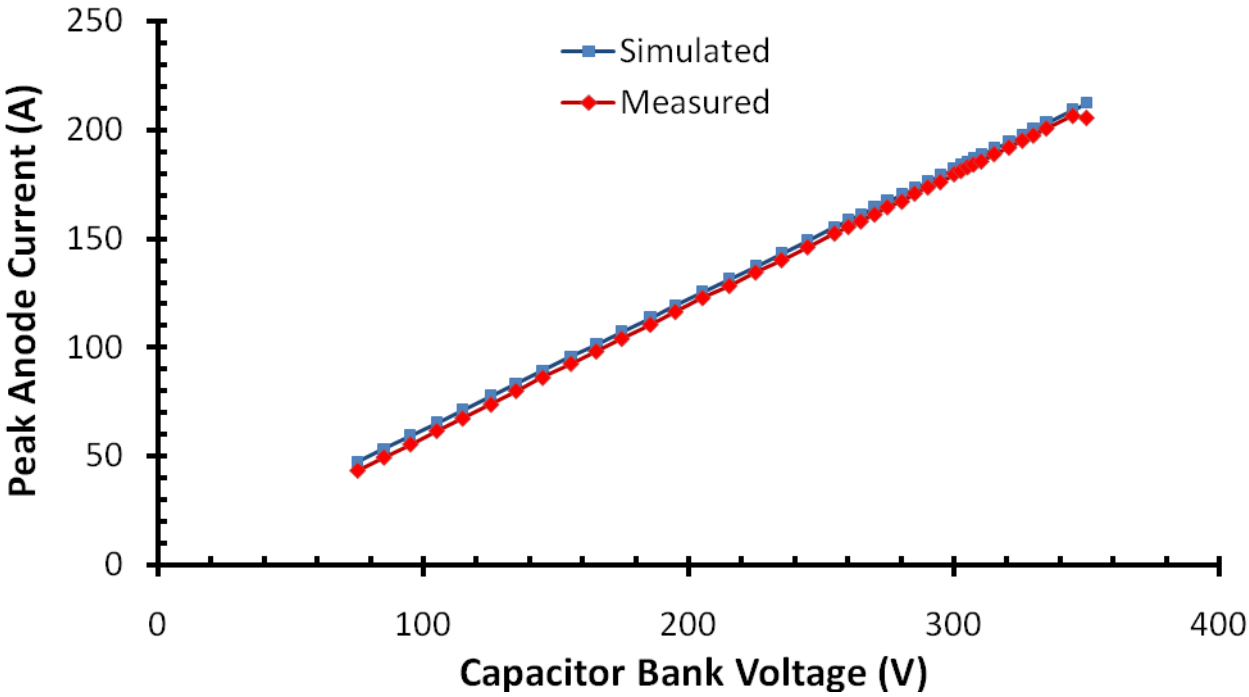


Figure 25: Rogowski Coil Verification

5 EXPERIMENTAL RESULTS

The second major part of the research project involved testing the GTO thyristors to investigate their turn-off characteristics. The investigation focused on how the peak turn-off gate current and snubber capacitance affected the turn-off characteristics of the GTOs. Special attention was given to determining the maximum interruptible current of the GTOs for various gate currents and snubber capacitances. A total of tweny-five identical GTO thyristors were tested to determine the various turn-off characteristics of the GTO thyristors.

5.1 Initial GTO Turn-off Characterization

Tests were initially conducted on the MGTO thyristors in order to gain a basic understanding of their specific turn-off characteristics. The goal of this cursory examination was to see how the gate turn-off current and snubber capacitance affected the turn-off characteristics of the GTO thyristors. The investigation did not seek to define a Safe Operating Area for the GTOs; rather it sought to gather additional data on the specific turn-off capabilities of the MGTO devices. This data was then used to focus the investigative efforts and make better use of the limited number of GTO thyristors.

The initial investigation collected a series of GTO thyristor turn-off waveforms. Each waveform recorded the voltage and current at the anode and gate of a GTO thyristor for a single turn-off switching event. The waveforms were collected using a four channel, digital oscilloscope (Tektronix TDS2024B) to measure and record the voltage and current at the gate and anode terminals of the GTO. For each switching event, the oscilloscope generated a numerical output file that contained all four channels of data and the time values corresponding to each data sample. The numerical output files were evaluated using a MATLAB® script to determine the turn-off anode current, the peak gate current, the turn-off gate charge, the anode voltage rise time, the current fall time, and the rate-of-change in the anode voltage and anode current. These values described the switching characteristics for the GTO thyristors for a particular combination of anode current, gate current, and snubber capacitance.

One representative set of GTO thyristor waveforms that was collected during the initial investigation is shown in Figure 26. The top graph shows the anode voltage (blue trace) and the anode current (maroon trace), while the bottom graph shows the gate voltage (blue trace) and the

gate current (maroon trace). This particular set of waveforms was collected when the GTO thyristors was used to interrupt ~200A of current; the GTO was turned off using a peak gate current of 45A and was protected by a 470nF snubber capacitor. The MATLAB® script (shown in Appendix D) used to analyze the waveforms shown in Figure 26 determined that the voltage rise time for the turn-off event was 880ns, the current fall time was 338ns, the rate of voltage rise was $317^{V}/_{\mu s}$, and the rate of current fall was $-475^{A}/_{\mu s}$.

From the graph it can be seen that the stray inductance in the snubber circuit is very small because there is no apparent spike in the anode voltage at the start of the turn-off transition (refer to Section 1.2). Additionally, the GTO thyristor was successfully able to interrupt a current pulse that was almost three times its 70A maximum interruptible current rating.

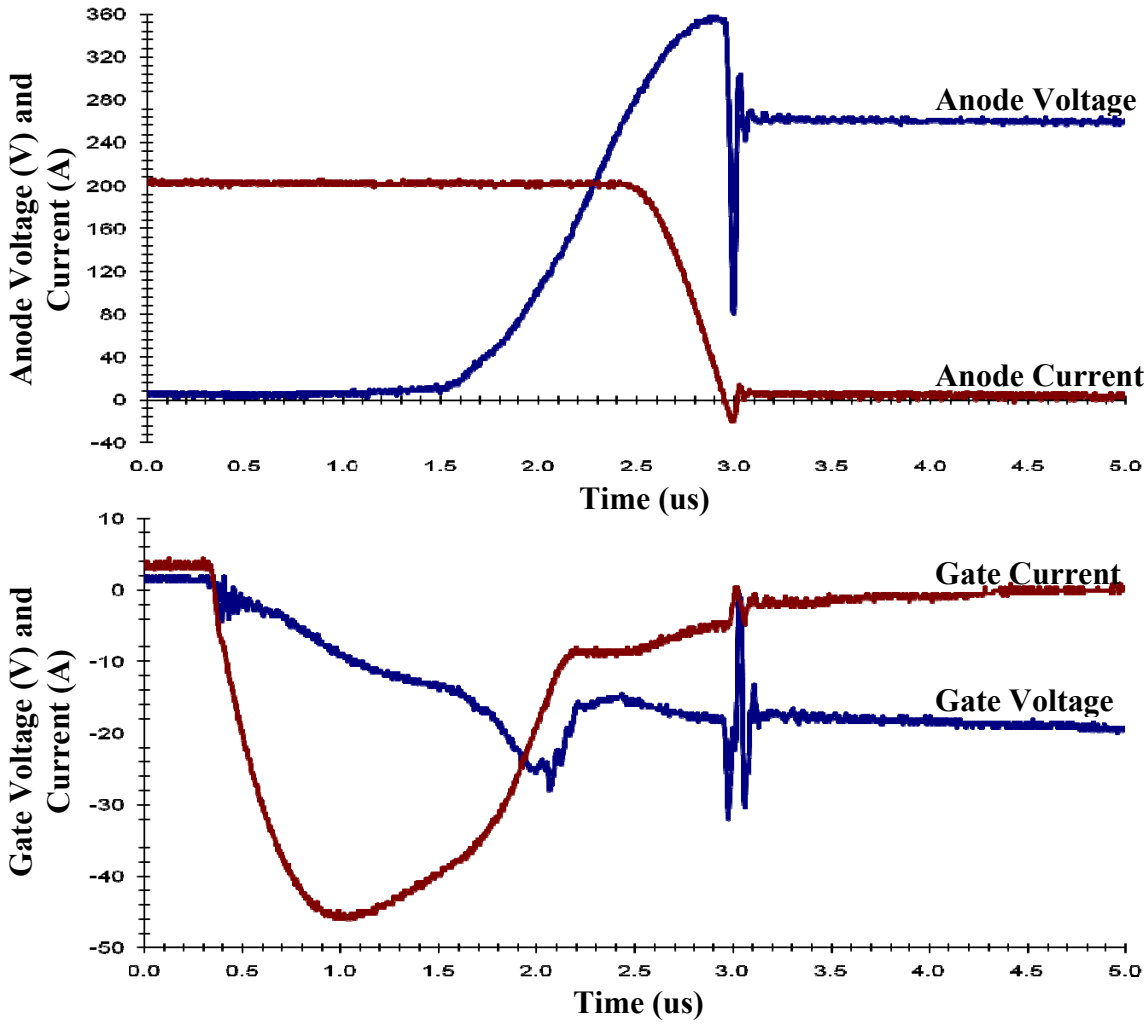


Figure 26: Experimental GTO Thyristor Waveforms

The initial investigation of the GTO thyristors showed that the gate current had a definite impact on the maximum interruptible current of the GTO thyristors. The snubber capacitance also affected the amount of current that the GTOs could turn off; however, its effect on maximum interruptible current was much less pronounced than the effect of the gate current. As a result of the initial investigation, it was decided to focus the majority of the remaining research efforts on examining the relationship between the gate current and the maximum turn-off capability of the GTO thyristors.

5.2 Minimum Gate Turn-off Current

Following the initial investigation of the GTO turn-off characteristics, five GTO thyristors were used to examine the minimum amount of gate current required to turn off the GTO thyristors. The same test methodoloy used in the initial investigation was used to determine the minimum turn-off gate current of the GTOs. The GTOs were used to interrupt specific levels of anode current, while the gate current was progressively reduced by lowering the voltage on the turn-off capacitor bank of the H-bridge gate driver. The graph in Figure 27 shows the overall result of the minimum gate curent examination; the diamonds show the gate currents that sucessfully turned off the GTOs while the X's indicate gate currents that failed to turn off the GTO thyristors.

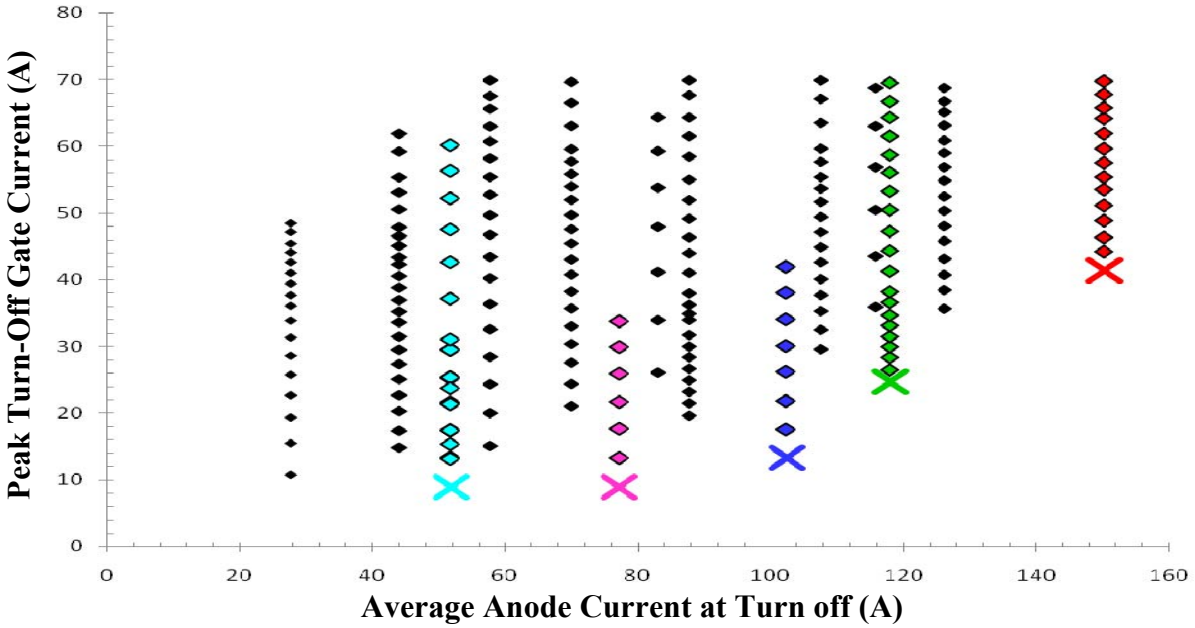


Figure 27: Minimum Gate Current

The plot shown in Figure 27 consolidates data taken from tests of the GTO thyristor at fourteen different anode currents. The red, green, blue, and magenta data points represent the first four test sequences; in those sequences, each GTO was tested at a different anode current using ever smaller gate turn-off current pulses until the device was not able to interrupt the anode current. These four sequences defined a rough Safe Operating Area (SOA) for the gate current of the GTO thyristors. (An SOA is the range of values in which a device will operate without failing.) A fifth GTO thyristor was used to verifiy the SOA defined by the previous four test sequence; the GTO was tested at ten different anode currents. For the first nine anode currents, represented by the small black diamonds in Figure 27, the gate current was always large enough to ensure safe turn-off of the GTO. For the final anode current value, the GTO was tested in the same way as the previous four GTOs; this sequence is represented by the cyan data points.

5.3 Maximum Interruptible Anode Current

The maximum interruptible current of the GTOs was tested using a set of twenty identical GTO thyristors. The test methodolgy remained fundamentally the same as in the previous investigations; the only difference was that the amount of gate current used to turn off the GTO thyristors was held constant for each test sequence while the anode current was increased until the GTOs were no longer able to turn off. (Remember from Section 2.2 that the peak anode current was controlled by the voltage on the high-voltage capacitor bank.) One additional factor that was considered in the testing of the maximum interruptible current was the amount of snubber capacitance used to protect the GTO thyristors during turn-off. To account for the effect of snubber capacitance on the turn-off current capacity, the GTO thyristors were divided into two groups and each tested with a different amount of snubber capacitance.

Figure 28 and Figure 29 show the overall results for the maximum interruptible current investigation (Figure 28 shows data for the GTOs tested using a 470nF snubber capacitor and Figure 29 shows data for the GTOs tested using a 940nF snubber capacitor.) Each vertical set of data points represents a specific test sequence in which a GTO thyristor was turned off using a constant gate current pulse for increasing amounts of anode current. The current at which the GTO thyristor failed to turn off is indicated by a large black X. It can be seen from the graph that the amount of gate current used to initiate device turn-off has a significant impact on the amount

of current that the GTO can interrupt. With enough gate current, the GTOs were able to interrupt almost three times their rated current interruption capacity (recall that the GTO thyristors were rated to interrupt 70A). The maximum amount of current that the GTOs were able to turn off was ~200A; this was because the devices had a 200A maximum surge current rating.

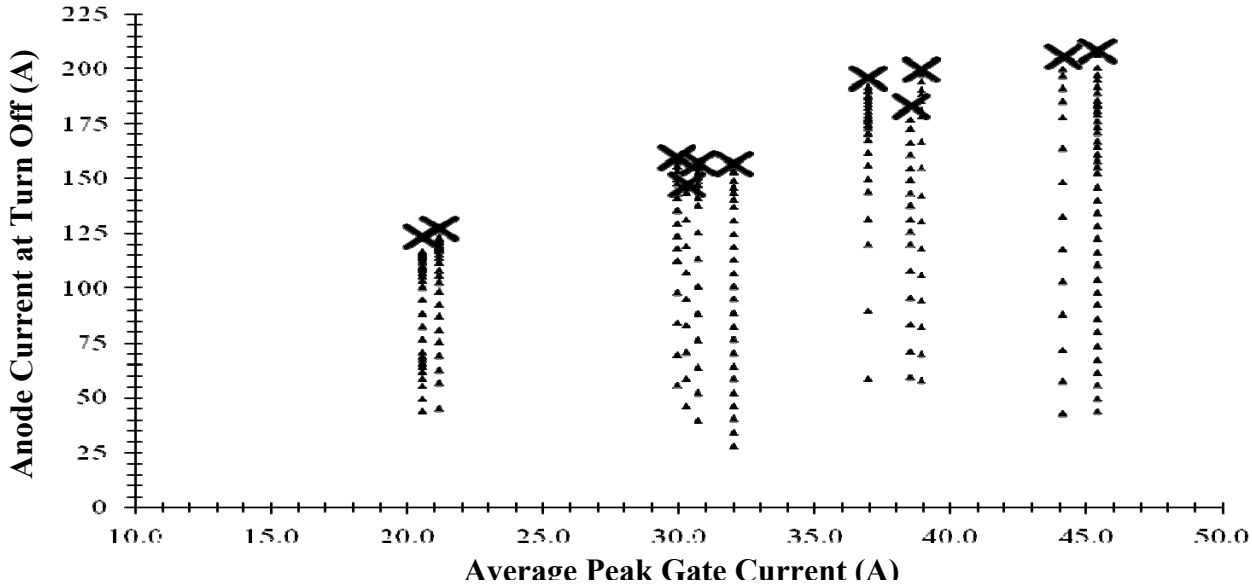


Figure 28: Maximum Interruptible Anode Current (470nF Snubber Capacitor)

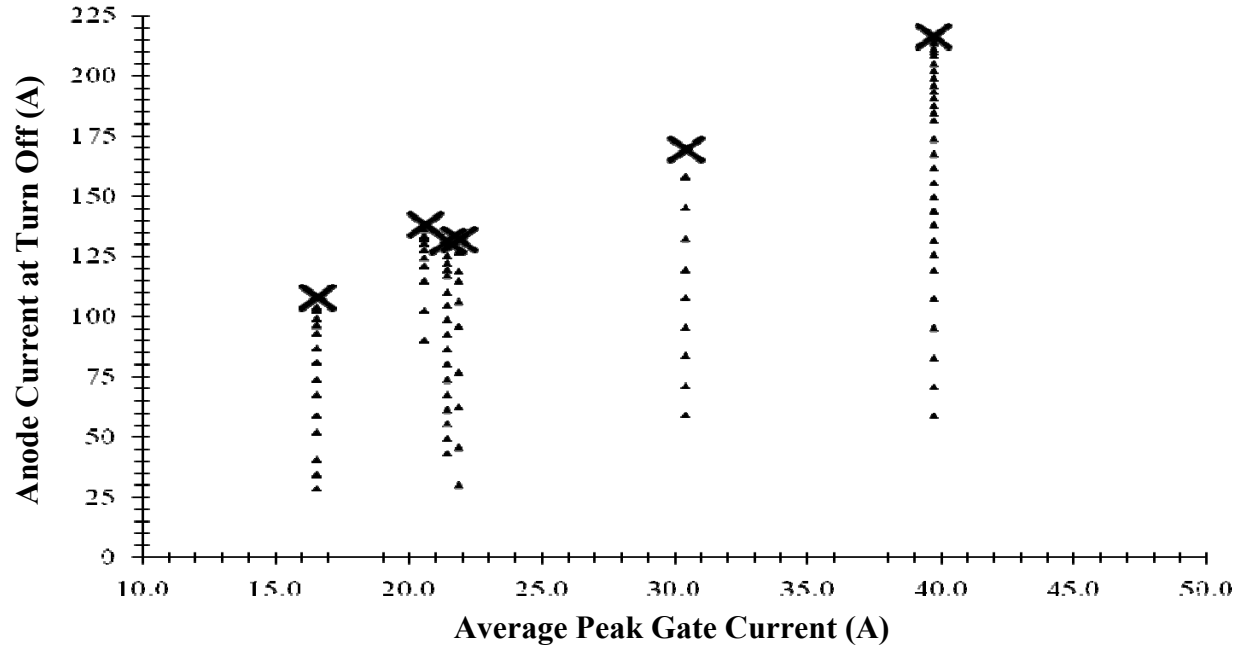


Figure 29: Maximum Interruptible Current (940nF Snubber Capacitor)

5.4 Safe Operating Area of the MGTO-1000 Thyristor

Using the data collected from the three test series, an overall Safe Operating Area (SOA) can be defined for the MGTO thyristor. Combining the minimum gate turn-off current data with the maximum interruptible current data allows an approximate SOA to be defined for the GTO thyristor at each snubber capacitance value. Figure 30 shows the approximate SOA for the GTOs when used to interrupt current with a 470nF snubber capacitor and Figure 31 shows the approximate SOA for the GTOs when used with a 940nF snubber capacitor. For both graphs, the SOA is represented by the shaded gray area.

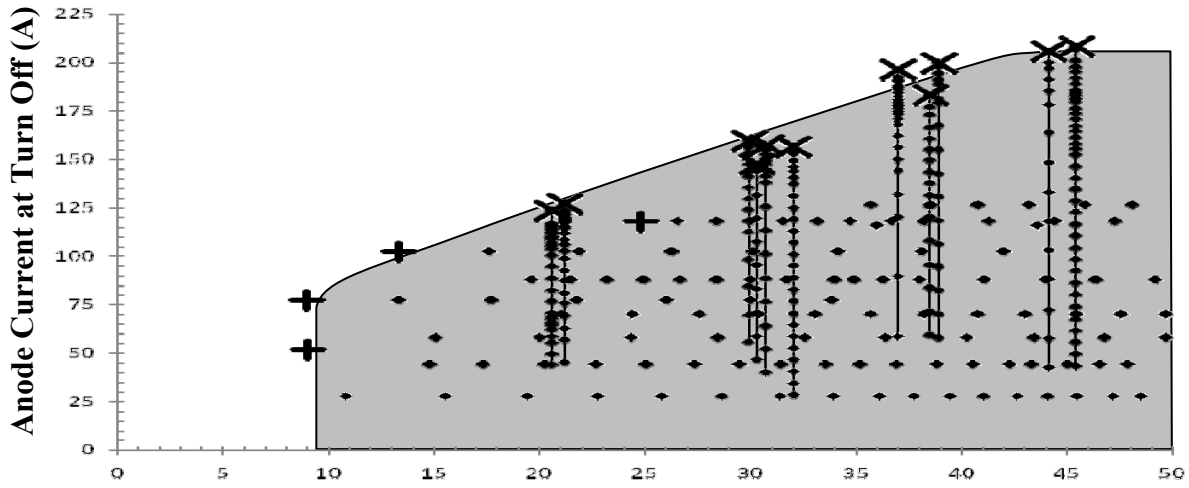


Figure 30: Approximate SOA (470nF Snubber Capacitor)

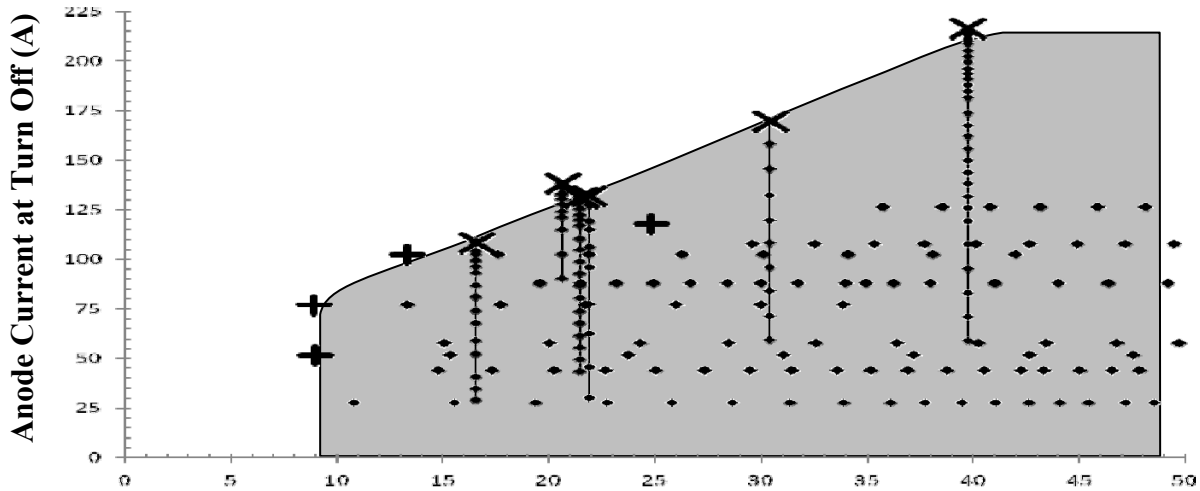


Figure 31: Approximate SOA (940nF Snubber Capacitor)

The two SOA's can be compared to examine the impact of the increased snubber capacitance on the current interruption capability of the GTO thyristors. Figure 32 shows the GTO SOA for both snubber capacitances. From the figure it can be seen that the increased snubber capacitance has very little impact on the current interruption capablity of the GTO thyristors in comparision to the effect of the gate turn-off current.

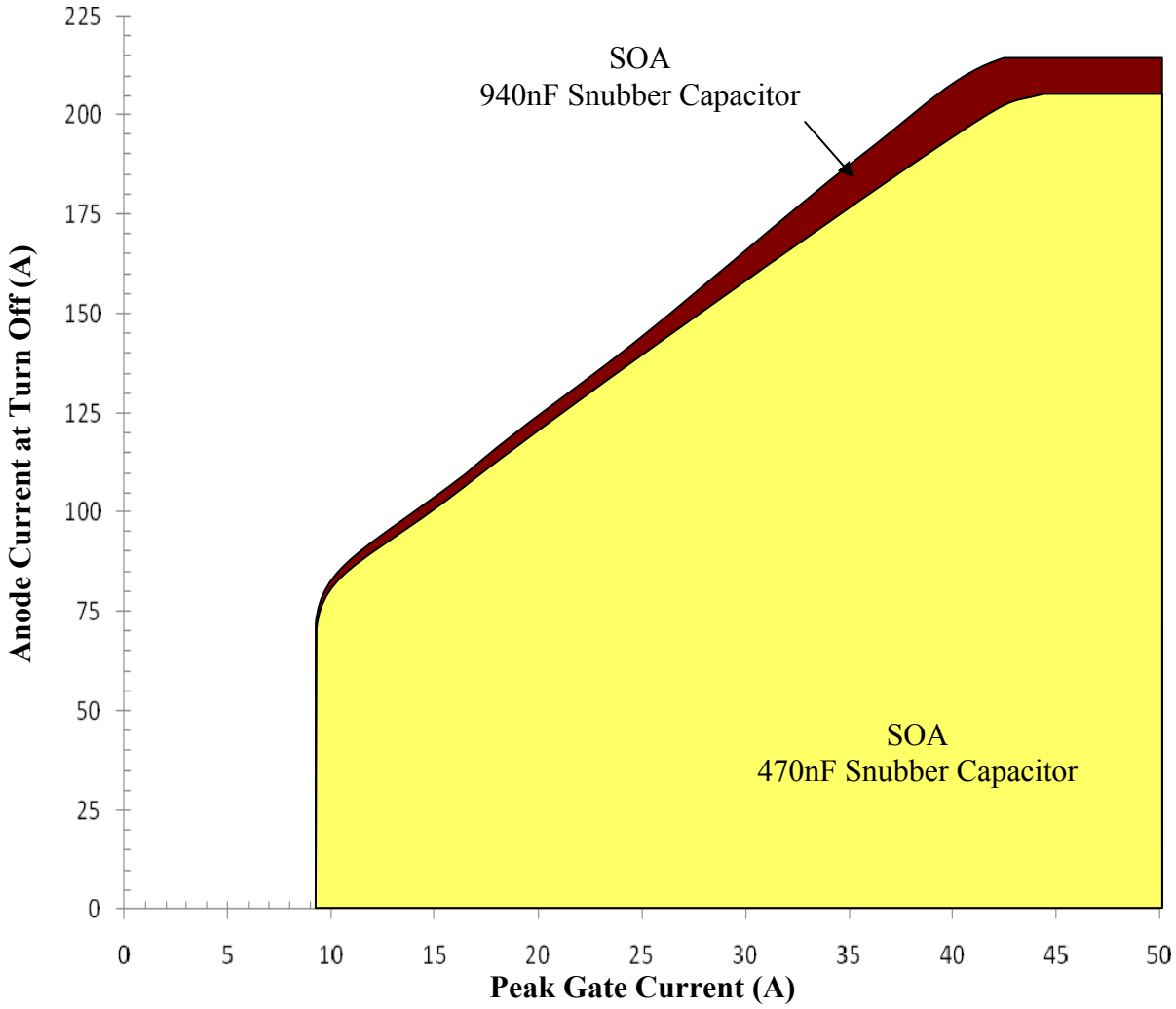


Figure 32: Safe Operating Area of GTO thyristor

6 CONCLUSIONS

This research project successfully demonstrated that GTO thyristors have a higher capacity for current interruption when they are used in a pulsed power source; confirming the IAT observation that GTOs in a pulse power source are capable of exceeding their maximum current interruption capability. This project went further by investigating the relationship between the turn-off gate current pulse and the current interruption capability of the GTOs; the effect of snubber capacitance on their current interruption capability was also investigated.

During this research effort, a test circuit was successfully designed to investigate the switching characteristics of a GTO thyristor in a pulse power application. The test circuit incorporated a fundamental resistor, inductor, capacitor (RLC) circuit to generate a switching "environment" similar to the inductive pulse forming network of a railgun system. The test circuit utilized an H-bridge gate drive circuit to generate the current pulses necessary to turn the GTO thyristors on and off. Finally, the test circuit utilized a Field Programmable Gate Array (FPGA) to control the timing of the H-bridge gate driver.

Implementation of the test circuit required significant experimental effort to determine the specific control requirements of the Motorola MGTO thyristor. Several modifications to the test circuit had to be made before the circuit could be utilized to investigate the turn-off characteristics of the MGTO thyristor. Additional effort was required to select and verify the instrumentation scheme to measure the voltage and current characteristics of the GTO thyristors during turn off. Particular care was made to measure the anode and gate currents without adding stray inductance to the test circuit.

Once the test circuit had been successfully implemented and verified, it was used to investigate the turn-off characteristics of twenty-five identical MGTO-1000 thyristors. The GTOs were used to interrupt anode currents that ranged from 50-220A using turn-off gate current pulses that ranged from 5A to 45A and two different snubber capacitance values. As the turn-off gate current pulse was increased, the amount of anode current that could be successfully interrupted by the GTO thyristors increased. The GTOs were able to successfully interrupt current values as high as their maximum surge current rating (almost three times their rated maximum interruptible current).

7 FUTURE WORK

There is a significant amount of future work that can follow from the findings of this project. The most immediate follow-on effort would be to repeat the project using larger GTO thyristors. As described previously, the MGTO thyristors were selected because they represented the best trade-off in terms of cost and current interruption capability. This research project has established that GTO thyristors do in fact have different switching capabilities when used in pulse power applications (as compared to the higher-frequency motor drive applications for which they are nominally rated); consequently, the cost of testing a batch of larger GTO thyristors (>$1000 per switch) would be more than justified.

Repeating this project using larger GTO thyristors would allow the "scalability" of GTO thyristors to be investigated. The current interruption capability of the GTOs investigated in this project was several orders of magnitude smaller than the GTO thyristors currently being considered for implementation in railgun pulse power sources. As a result, the trend between gate current and maximum interruptible current capability needs to be examined using the high current GTO thyristors.

Another potential area of future effort would be to modify the test circuit to investigate the effect of switching frequency on the current interruption capability of the GTO thyristors. The test circuit used in this project designed to perform one switch test at a time; however, the control code and high voltage power supply could be easily modified to perform multiple switch tests at a regular repetition rate (rep-rate). Ultimately, the goal of the rep-rate investigation would be to evaluate the current interruption capability of GTO thyristors at the expected rep-rate of a military railgun application (6-12 repetitions per minute).

One final area of future effort would be to investigate the effect of conduction time on the current interruption capability of GTO thyristors. In this project, the GTO thyristors were always turned off after 5ms of conduction; this insured that the current pulse did not exceed the maximum fusing rating of the MGTO thyristor. In many inductor based pulsed power sources, the charging current pulse lasts significantly longer than 5ms, so it is important to determine how longer conduction times will affect a GTO's current interruption capability.

APPENDIX A: RAILGUN PULSE POWER SOURCES

Railgun systems typically employ one of three potential pulsed power sources: capacitive pulse forming networks, inductive pulse forming networks, and compulsators. A capacitive pulse forming network stores up the energy for the output current pulse as electric potential within banks of capacitors. Inductive pulse forming networks store up the energy for the output current pulse in the magnetic field of large inductors. Compulsators store up energy as kinetic energy in the rotational inertia of a high-speed rotating disk and use a pulsed alternator to convert the kinetic energy into short pulses of current.

Probably the most common pulse power source used with modern railguns is the capacitive pulse forming network. Capacitive pulse forming networks (CPFNs) are relatively easy to design and construct and do not require complex expensive components. Figure 33 shows the circuit diagram of a simple four-stage capacitive pulse forming network; each stage consists of a capacitor bank, a small inductor, and a power switch. (The power switches are modeled in Figure 33 as an ideal switch in series with a diode.)

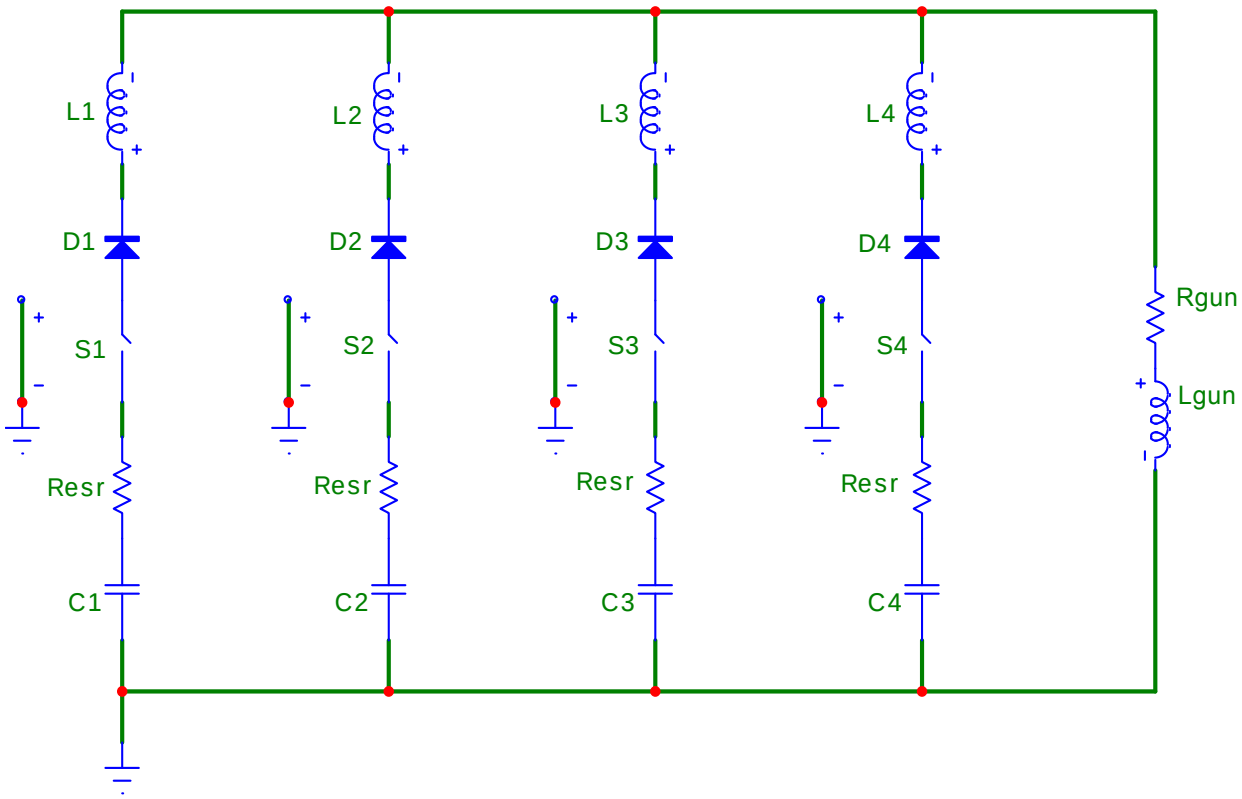


Figure 33: Four-Stage Capacitive Pulse Forming Network

Capacitive pulse forming networks generate current pulses by "ripple-firing" a series of capacitor banks into the railgun. Each capacitor bank is connected to the railgun by a power switch and an inductor. The switches determine when each capacitor bank discharges into the railgun and the inductors act as pulse formers to force each capacitor to discharge with a quasi-sinusoidal current pulse. The plot in Figure 34 shows the sequence of current pulses that are generated by the discharging capacitor banks as each power switch turns on.

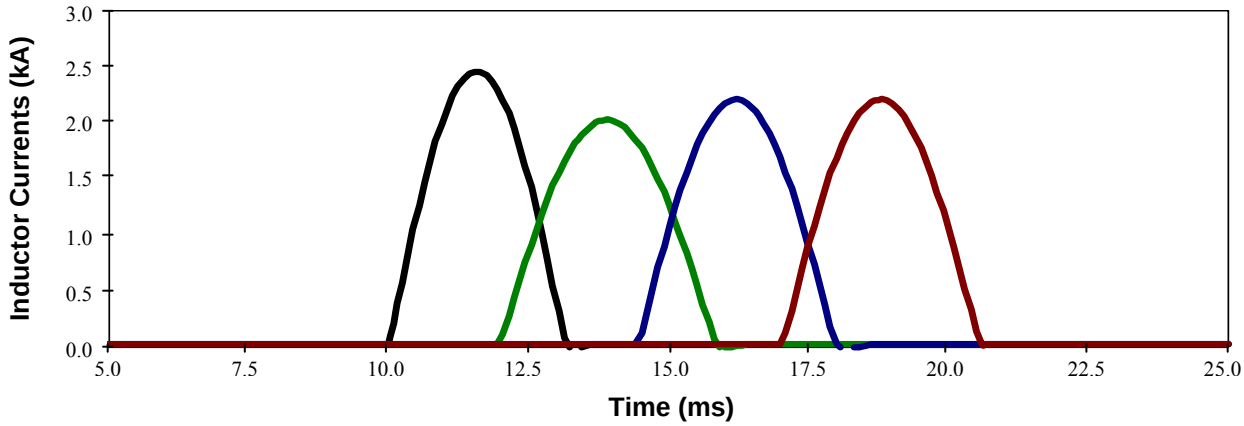


Figure 34: Capacitor Bank Discharge Currents
Plot Traces from Left to Right: I(C1), I(C2), I(C3), I(C4)

The individual current pulses that are generated by each stage of the capacitive pulse forming network combine to generate the overall output pulse. The shape of the output current pulse is determined by the switch timing and by the size of the pulse shaping inductors. As shown in Figure 35, proper switch timing and pulse shaping inductances can allow a capacitive pulse forming network to generate a nearly trapezoidal current pulse.

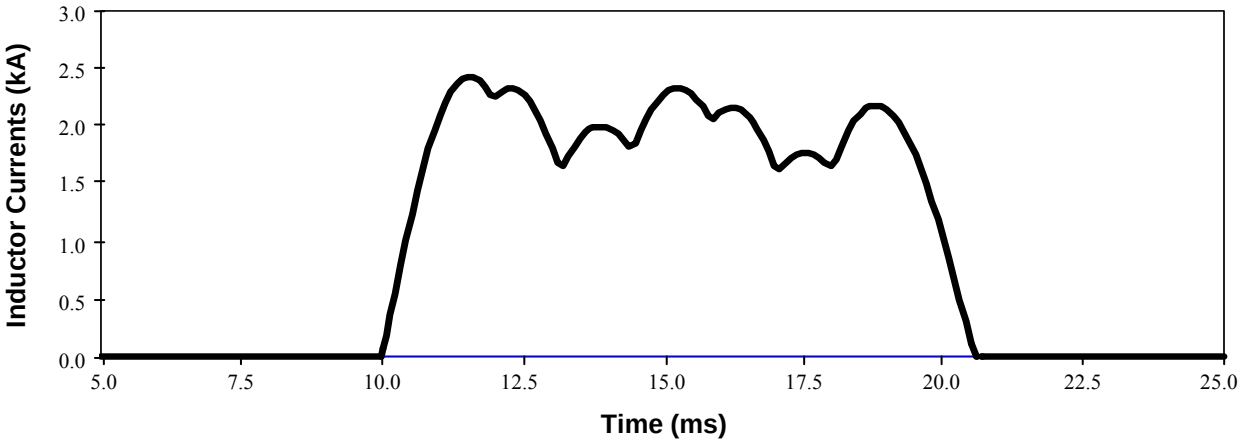


Figure 35: Overall Output Current from Capacitive Pulse Forming Network

Capacitive pulse forming networks see widespread use because they can be constructed using fairly simple power electronic components. Because the power switches only have to close (i.e. turn on), they can be easily implemented with solid-state components like Silicon Controlled Rectifiers (SCRs) or power thyristors. Additionally, the overall pulse shape is easy to change by adjusting the switch timing, the size of the pulse shaping inductors, and the initial voltages on the capacitor banks. The primary disadvantage of capacitive pulse forming networks is the poor energy density of capacitors ($10MJ/m^3$).[21] At present, capacitor banks are prohibitively large to be used in shipboard railgun weapon systems.

One possible solution (more of a workaround) to the poor energy density of capacitors is to construct a pulse forming network which uses inductors to store the energy required for the output pulse. Currently, inductive energy storage has a higher energy density than capacitive energy storage ($50MJ/m^3$)[20]; however, the increasing prevalence of super-capacitors may allow capacitive energy storage to surpass the energy density of inductive energy storage in the near future. Furthermore, inductive pulse forming networks tend to be more complex and harder to implement than capacitive pulse forming networks. Consequently, inductive pulse forming networks are typically not the first choice of researchers in the railgun arena.

Fundamentally an inductive pulse forming network consists of two current loops with the storage inductor(s) common to both loops. One of the loops contains the external power supply and is used to charge up the storage inductor(s), the other loop contains the railgun through which the storage inductor(s) are discharged. The actual operation, aka "firing," of an inductive pulse forming network is controlled by the switch that connects the external power supply to the storage inductors. Closing the switch connects the external power supply to the storage inductors and initiates charging; opening the switch connects the storage inductors to the railgun, causing the discharge of current through the railgun armature (projectile).

Figure 36 shows the circuit diagram of an inductive pulse forming network developed by the Institute for Advanced Technology (IAT-UT) that uses a pair of storage inductors.[22] The GTO thyristor controls the charging and discharging of the storage inductors L1 and L2. The external DC power supply is represented by the component V1 and the railgun is represented by the resistance Rgun and the inductance Lgun.

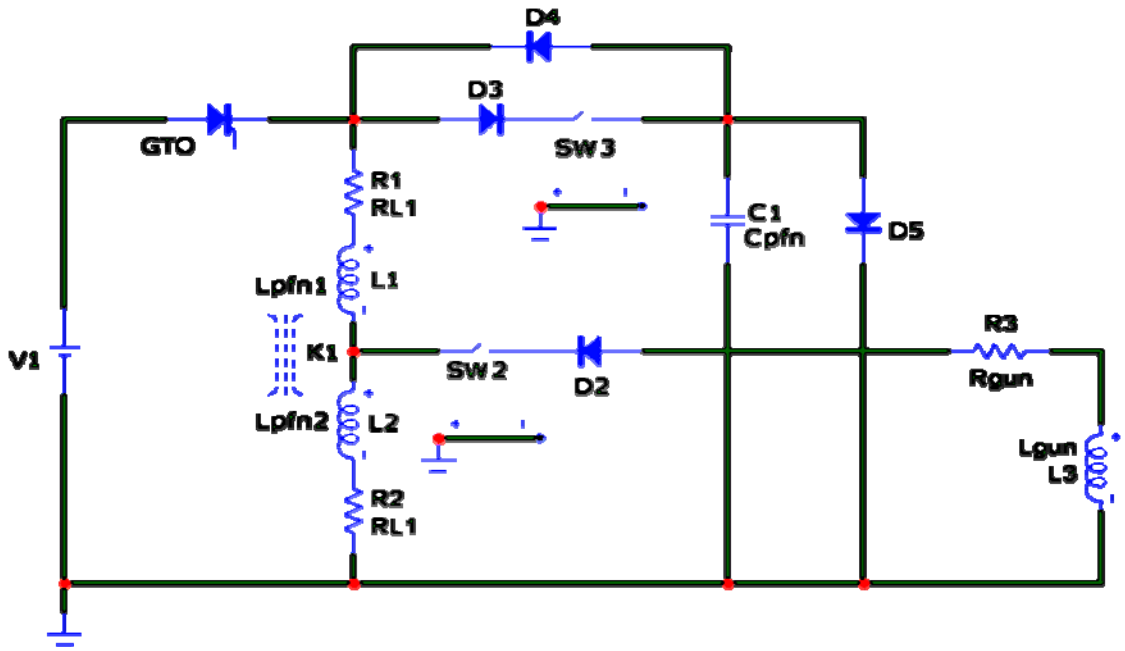


Figure 36: STRETCH Meat Grinder Inductive Pulse Forming Network

To charge up the inductive pulse forming network, the GTO turns on to allow the external power supply V1 to generate current in the storage inductors. Ideally the inductor current will linearly build to some target level; since the energy stored in an inductor is proportional to the square of the inductor current, the external power supply can store a significant amount of energy in the inductors. To "fire" the inductive pulse forming network, the GTO has to turn off to interrupt the current path between the external power supply and the storage inductors. When the GTO opens to interrupt the charging loop, it transfers or "commutates" the current in the inductors to the railgun loop in order to initiate the output current pulse.

It is extremely difficult to interrupt high current levels, especially if the current is through an inductor. At present, explosive opening switches are the most commonly employed method of interrupting high currents; unfortunately, these switches can only be used once before they destroy themselves. The voltage across an inductor depends upon the rate change of current through the inductor ($V = L\frac{dI}{dt}$). In inductive pulse forming networks, a large spike in the voltage across the storage inductors occurs when the switch (labeled GTO in Figure 36) interrupts the charging loop to initiate the output current pulse. Consequently, the energy capacity

(proportional to the maximum inductor current) of an inductive pulse forming network is limited by the amount of current that the switch can interrupt. High energy inductive pulse forming networks need robust turn-off (aka "opening") switches. Unfortunately, existing switch technologies are not robust enough to allow inductive pulse forming networks to match the energy capacity of large capacitive pulse forming networks.

The inductive pulse forming network shown in Figure 36 has some additional circuit components that shape the output current pulse. The switch SW2 closes just before the GTO opens. Consequently, the current in inductor L1 cannot commutate to the railgun after the GTO opens. Since the two storage inductors are coupled, the abrupt interruption of current in the inductor L1 allows some of the energy stored in the inductor L1 to transfer to the inductor L2 and causes the current in the inductor L2 to rise. Figure 37 shows how the current in the inductor L1 (dotted line) rapidly drops to zero while the current in the inductor L2 (solid line) increases.

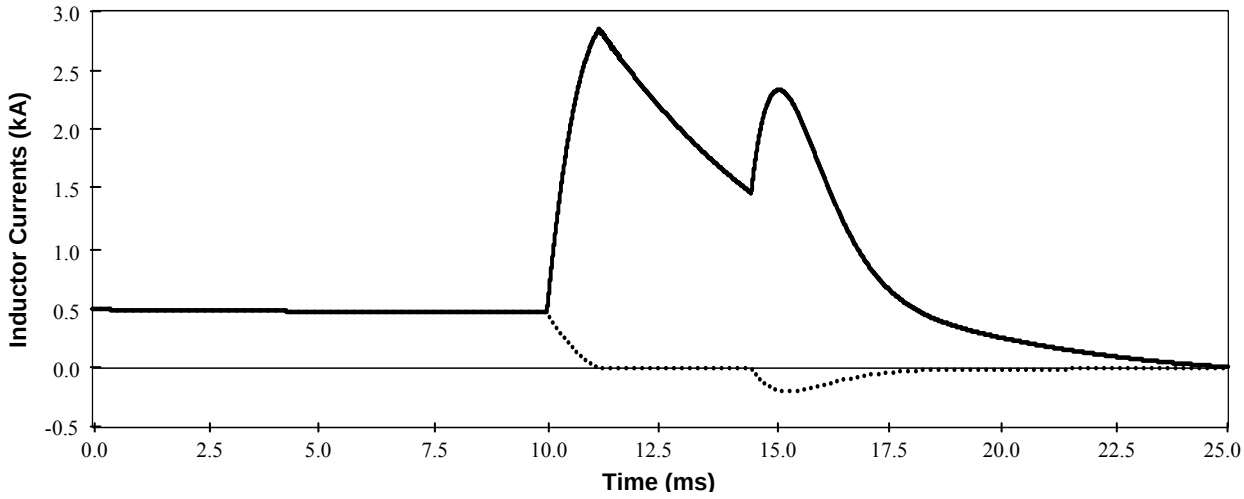


Figure 37: Inductor Currents in an Inductive Pulse Forming Network

As the current in the inductor L1 rapidly decays to zero, the voltage across the storage inductors rapidly increases. Instead of damaging the opening switch (GTO), the spike in voltage across the inductor charges up the capacitor C1 (the capacitor limits the overall magnitude of the voltage spike). After the current in the inductor L1 reaches zero and the capacitor is fully charged, the switch SW3 closes to discharge the capacitor into the railgun and back through the inductor L1. As shown in Figure 37, when the capacitor C1 discharges it creates a second current pulse in the inductor L1. Since the two inductors are coupled, the current pulse in the inductor L1 causes the current in the inductor L2 to increase for a second time.

The shape of the overall output current pulse depends primarily on the size and resistance of the two storage inductors. However, the capacitor size and capacitor discharge delay time can be chosen to improve the overall shape of the output current pulse. Figure 38 shows the overall output current that resulted from the inductor currents shown in Figure 37. The first current peak is generated by the energy discharge from the two storage inductors while the second current peak is generated by the energy discharge of the capacitor. The plot was generated by simulating the inductive pulse forming network shown in Figure 36. The inductance of the first inductor (L1) was 2mH, the inductance of the second inductor (L2) was 50uH, the capacitance of the capacitor (C1) was 2mF, and the current in the inductors was 500A when the switch opened to initiate the output pulse.

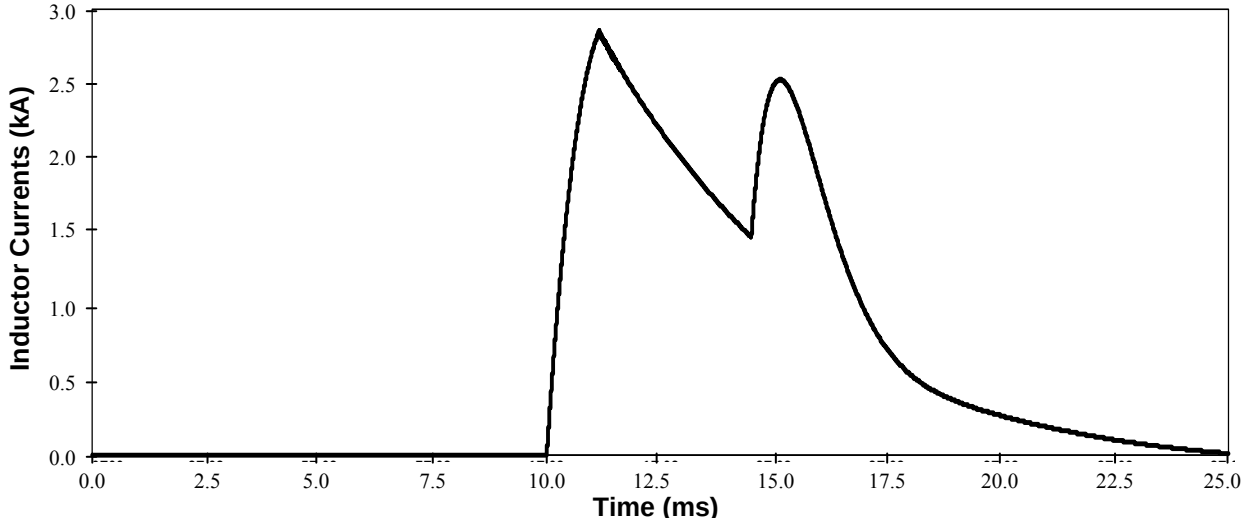


Figure 38: Output Current from an Inductive Pulse Forming Network

The inductive pulse forming network developed by IAT and shown in Figure 36 is known as a STRETCH meatgrinder pulse inductive pulse forming network because of its unique circuit topology. The switches SW2 and SW3 allow more energy to be "squeezed" out of the two inductors than would be possible by simply discharging the inductors into the railgunt

Both capacitive pulse forming networks and inductive pulse forming networks have major disadvantages. Capacitive pulse forming networks are prohibitively large for use in a shipboard railgun weapon system while inductive pulse forming networks cannot meet the energy requirements. A third type of pulsed power source, known as a compensated pulsed alternator (compulsator), might actually provide the ultimate solution to the Navy's pulse power

requirements. Compulsators use a high-speed spinning disk to store up kinetic energy. Compulsators use a pulsed alternator to convert the kinetic energy stored in the rotational inertia of the disk into electrical energy in the form of a short pulse of high-current. At present, compulsators have the highest energy density of the three types of pulse power sources (>100MJ/m^3).[20] However, the Navy is cautious of the added complexity and safety concerns inherent to a pulsed power source that incorporates both mechanical and electrical components.

At present, the Navy is researching all three approaches to energy storage. The Navy has an Electromagnetic Rail Launch Facility (EMLF) at Naval Surface Warfare Center Dahlgren Division (N.S.W.C.D.D.) that uses a capacitive pulse forming network to fire a 10 meter research launcher. The pulse forming network has 11 different capacitor banks and can store up 41MJ of total energy. The railgun launcher fires a 3-inch projectile and can achieve muzzle velocities approaching 2500 meters per second (approximately 8-10MJ of muzzle energy).[23] Both the Navy and the Army support railgun research at the University of Texas Institute for Advanced Technology. IAT-UT is currently constructing a STRETCH meat grinder inductive pulse forming network to power a 1 meter rail launcher. The pulse forming network will store approximately 28kJ of energy in the inductors and allow the railgun to achieve muzzle energies approaching 4kJ.[24]

APPENDIX B: VHDL CONTROL CODE

```
--------------------------------------------------------------------------------------------------
--  GATE DRIVER CONTROL LOGIC                                                                   --
--                                                                                              --
--  TRIDENT RESEARCH PROJECT:  Opening Switch Characterization                                  --
--  Advisors:  Dr. Ciezki                                                                       --
--             Dr. Salem                                                                        --
--                                                                                              --
--  Author:    Gerald Vineyard                                                                  --
--             Midshipman, USN                                                                  --
--                                                                                              --
--  Location:  United States Naval Academy                                                      --
--  Date:      13 January 2008                                                                  --
--                                                                                              --
--  Function:  This program serves as the control logic for the GTO gate driver in              --
--             the test circuit.  This program will be used in the ALTERA DE2                   --
--             Demonstration Board to control the bridge driver that operates the               --
--             gate circuit of the GTO.                                                         --
--------------------------------------------------------------------------------------------------

LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_unsigned.all;
USE ieee.std_logic_arith.all;

ENTITY GateDriverCyclone IS
        PORT (
                -- Clock Input --
                CLOCK_50MHZ     :       in std_logic;           -- 50 MHz Clock

                -- Switch Inputs --
                switch          :       in std_logic_vector(17 downto 0);   -- Toggle Switches

                -- Button Inputs --
                button          :       in std_logic_vector(3 downto 0);    -- Button

                -- LCD Module Control Values --
                LCD_DATA        :       inout std_logic_vector(7 downto 0); -- LCD Data Bus
                LCD_ON          :       out std_logic;                      -- LCD Power
                LCD_BLON        :       out std_logic;                      -- LCD Back Light
                LCD_EN          :       out std_logic;                      -- LCD Enable
                LCD_RW          :       buffer std_logic;               --  LCD Read/Write Select
                LCD_RS          :       out std_logic;          -- LCD Command/Data Select:
```

```
		-- LEDR Outputs --
		ledr		:	out std_logic_vector(17 downto 0);		-- Red LEDs
		ledg		:	out std_logic_vector(8 downto 0);		-- Green LEDs

		-- 7 Segment Displays --
		hex0		:		out std_logic_vector(7 downto 0);	-- Digit 0
		hex1		:		out std_logic_vector(7 downto 0);	-- Digit 1
		hex2		:		out std_logic_vector(7 downto 0);	-- Digit 2
		hex3		:		out std_logic_vector(7 downto 0);	-- Digit 3
		hex4		:		out std_logic_vector(7 downto 0);	-- Digit 4
		hex5		:		out std_logic_vector(7 downto 0);	-- Digit 5
		hex6		:		out std_logic_vector(7 downto 0);	-- Digit 6
		hex7		:		out std_logic_vector(7 downto 0);	-- Digit 7

		GPIO		:		inout std_logic_vector(35 downto 0)  -- Control
		);
END GateDriverCyclone;



ARCHITECTURE logic OF GateDriverCyclone IS
	TYPE mode	IS (FIRE, TIME_SET);
	TYPE disp	IS (PW_ON, PW_OFF, DELAY_ON, DELAY_OFF, VALID_ENABLE);
	TYPE setV	IS (SEC, mSEC, uSEC, HOLD);
	TYPE lcd	IS (FUNC_SET, DISPLAY_ON, DISPLAY_OFF, DISPLAY_CLEAR,
			RESET, FIRST_LINE_MODE, SECOND_LINE_MODE,  NEW_LINE,
			RETURN_ORIGIN, TOGGLE_E, HOLD, CHAR1, CHAR2, CHAR3,
			CHAR4, CHAR5, CHAR6, CHAR7, CHAR8, CHAR9, CHAR10,
			CHAR11, CHAR12, CHAR13, CHAR14, CHAR15, CHAR16, CHAR17,
			CHAR18, CHAR19, CHAR20, CHAR21, CHAR22, CHAR23, CHAR24,
			CHAR25, CHAR26, CHAR27, CHAR28, CHAR29, CHAR30, CHAR31,
			CHAR32);

	-- Functional States:  LCD Display, Time Set, and Program Mode --
	SIGNAL current_LCD		:	lcd	:= RESET;
	SIGNAL next_LCD			:	lcd;
	SIGNAL current_state		:	mode;
	SIGNAL next_state		:	mode;
	SIGNAL current_display		:	disp	:= VALID_ENABLE;
	SIGNAL next_display		:	disp	:= VALID_ENABLE;
	SIGNAL current_value		:	setV;
	SIGNAL next_value		:	setV;
```

```
-- Clock Divider Values --
SIGNAL CLK_COUNT_1kHZ       : STD_LOGIC_VECTOR(19 DOWNTO 0) :=  X"00000";
SIGNAL CLK_1kHZ             : STD_LOGIC                      := '0';
SIGNAL CLK_COUNT_1MHZ       : STD_LOGIC_VECTOR(7 DOWNTO 0)   := X"00";
SIGNAL CLK_1MHZ             : STD_LOGIC                      := '0';

-- LCD Display Characters --
SIGNAL M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16,
       M17, M18, M19, M20, M21, M22, M23, M24, M25, M26, M27, M28, M29, M30,
       M31, M32,
LCD_DATA_VALUE              : STD_LOGIC_VECTOR(7 DOWNTO 0);

-- Timing Buffer for Driver Circuitry Initialization
SIGNAL initialize           :       std_logic_vector(15 downto 0)       := X"0000";
SIGNAL initDelay            :       std_logic_vector(15 downto 0)       := X"1388";
SIGNAL lowSideOn            :       std_logic_vector(15 downto 0)       := X"03E8";
SIGNAL lowSideOff           :       std_logic_vector(15 downto 0)       := X"0FA0";

-- Time from experiment initiation to switch Turn On pulse --
SIGNAL OnDelay_sec          :       integer range 0 to 999          := 0;
SIGNAL OnDelay_msec         :       integer range 0 to 999          := 0;
SIGNAL OnDelay_usec         :       integer range 0 to 999          := 0;
SIGNAL OnDelay              :       std_logic_vector(31 downto 0) := X"00000000";

-- Time from experiment initiation to switch Turn Off pulse --
SIGNAL OffDelay_sec         :       integer range 0 to 999          := 0;
SIGNAL OffDelay_msec        :       integer range 0 to 999          := 0;
SIGNAL OffDelay_usec        :       integer range 0 to 999          := 0;
SIGNAL OffDelay             :       std_logic_vector(31 downto 0) := X"00000000";

-- Pulse Width of Turn On pulse --
SIGNAL OnPW_sec             :       integer range 0 to 999          := 0;
SIGNAL OnPW_msec            :       integer range 0 to 999          := 0;
SIGNAL OnPW_usec            :       integer range 0 to 999          := 0;
SIGNAL OnPW                 :       std_logic_vector(31 downto 0) := X"00000000";

-- Pulse Width of Turn Off pulse --
SIGNAL OffPW_sec            :       integer range 0 to 999          := 0;
SIGNAL OffPW_mse            :       integer range 0 to 999          := 0;
SIGNAL OffPW_usec           :       integer range 0 to 999          := 0;
SIGNAL OffPW                :       std_logic_vector(31 downto 0) := X"00000000";

-- Time Value for Overal Experiment --
SIGNAL exp_Time             :   std_logic_vector(63 downto 0) := X"0000000000000000";
```

```
        -- Binary Vectors For Current Display Output --
        SIGNAL secHundred               :       std_logic_vector(3 downto 0)  := X"0";
        SIGNAL secTen                   :       std_logic_vector(3 downto 0) := X"0";
        SIGNAL secOne                   :       std_logic_vector(3 downto 0) := X"0";
        SIGNAL millisecHundred          :       std_logic_vector(3 downto 0)  := X"0";
        SIGNAL millisecTen              :       std_logic_vector(3 downto 0)  := X"0";
        SIGNAL millisecOne              :       std_logic_vector(3 downto 0)  := X"0";
        SIGNAL microsecHundred          :       std_logic_vector(3 downto 0)  := X"0";
        SIGNAL microsecTen              :       std_logic_vector(3 downto 0)  := X"0";
        SIGNAL microsecOne              :       std_logic_vector(3 downto 0)  := X"0";

        -- Safety Interlocks --
        SIGNAL valid_timing             :       std_logic       := '0';
        SIGNAL system_enable            :       std_logic       := '0';

        -- Experiment Control Signals --
        SIGNAL start_experiment         :       std_logic       := '0';
        SIGNAL end_experiment           :       std_logic       := '0';

        -- Control Ouptuts --
        SIGNAL OnLow                    :       std_logic       := '0';
        SIGNAL OnHigh                   :       std_logic       := '0';
        SIGNAL OffLow                   :       std_logic       := '0';
        SIGNAL OffHigh                  :       std_logic       := '0';
        SIGNAL Disable                  :       std_logic       := '0';

BEGIN
        ------------------------------------------------------------------------------------------------
        -- Controls the Switch Inputs to the logic function.  Four of the switches are used as a –
        -- combination of mode select (Time_Set or Fire) and safety interlock.  The only way –
        -- for the function to actually output the switch control pulses is for all four timing     --
        -- values to be valid and all four interlock switches to be correctly aligned.               --
        ------------------------------------------------------------------------------------------------
process(switch)
        begin
                if (switch(17) = '1' AND switch(16) = '1') then
                        current_state <= FIRE;
                        hex6 <= X"2B";
                        hex7 <= X"23";
                else
                        current_state <= TIME_SET;
                        hex6 <= X"7F";
                        hex7 <= X"7F";
                end if;
```

```
        if (switch(15:14) = “00” AND switch(13:12) = “11”) then
                system_enable <= '1';
        else
                system_enable <= '0';
        end if;


        if (switch(17 downto 12) = "110011") then
                hex4 <= X"2B";
                hex5 <= X"23";
        else
                hex4 <= X"7F";
                hex5 <= X"7F";
        end if;
end process;
```

```
-------------------------------------------------------------------------------------------------
-- Process allows user to toggle through set values and display screens using the    --
-- push buttons.                                                                     --
-------------------------------------------------------------------------------------------------
process(button, current_state, end_experiment)
begin
        if (button(0)'EVENT AND button(0) = '1') then
                current_display <= next_display;
        else
                null;
        end if;

        if (current_state = FIRE OR current_display = VALID_ENABLE) then
                current_value <= hold;
        else
                if (button(1)'EVENT AND button(1) = '1') then
                        current_value <= next_value;
                else
                        null;
                end if;
        end if;
```

```
		if (current_state = FIRE AND system_enable = '1' AND valid_timing = '1' AND
end_experiment = '0') then
			if(button(2)'EVENT AND button(2) = '1') then
				start_experiment <= '1';
			else
				null;
			end if;
		else
			start_experiment <= '0';
		end if;
	end process;


	-------------------------------------------------------------------------------------------------------
	-- Bridge Driver Control Logic:
	--	Outputs Five Logic Signals Based On the Program State and the 1MHz Clock Input
	-------------------------------------------------------------------------------------------------------
	process (CLK_1MHZ)
	begin
		if (start_experiment = '1' AND end_experiment = '0') then
			Disable <= '0';

			if (CLK_1MHZ'EVENT AND CLK_1MHZ = '1') then
				if (initialize < initDelay) then
					initialize <= initialize + 1;
				else
					exp_Time <= exp_Time + 1;
				end if;
			else
				null;
			end if;

			if (initialize < initDelay) then
				if (initialize > lowSideOn AND initialize < lowSideOff) then
					OnLow <= '1';
					OnHigh <= '0';
					OffLow <= '1';
					OffHigh <= '0';
				else
					OnLow <= '0';
					OnHigh <= '0';
					OffLow <= '0';
					OffHigh <= '0';
				end if;
```

```
                else
                        if (exp_Time < OnDelay) then
                                OnLow <= '0';
                                OnHigh <= '0';
                                OffLow          <= '0';
                                OffHigh <= '0';
                        elsif (exp_Time > OnDelay AND exp_Time < OnDelay + OnPW) then
                                OnLow <= '1';
                                OnHigh <= '1';
                                OffLow          <= '0';
                                OffHigh <= '0';
                        elsif (exp_Time > OnDelay + OnPW AND exp_Time < OffDelay) then
                                OnLow <= '0';
                                OnHigh <= '0';
                                OffLow          <= '0';
                                OffHigh <= '0';
                        elsif (exp_Time > OffDelay AND exp_Time < OffDelay + OffPW) then
                                OnLow <= '0';
                                OnHigh <= '0';
                                OffLow          <= '1';
                                OffHigh <= '1';
                        else
                                OnLow <= '0';
                                OnHigh <= '0';
                                OffLow          <= '0';
                                OffHigh <= '0';
                        end if;
                end if;
        else
                Disable <= '1';
                OnLow <= '0';
                OnHigh <= '0';
                OffLow          <= '0';
                OffHigh <= '0';
                exp_Time <= X"0000000000000000";
                initialize <= X"0000";
        end if;
end process;
```

```
	-----------------------------------------------------------------------------------------------
	-- Clock Divider: Generates a 1MHz 50% Duty Cycle Signal                                      --
	-----------------------------------------------------------------------------------------------
	process (CLOCK_50MHZ)
	begin
		if (CLOCK_50MHZ'EVENT AND CLOCK_50MHZ = '1') then
			if (CLK_COUNT_1MHZ < X"19") then
				CLK_COUNT_1MHZ <= CLK_COUNT_1MHZ + 1;
			else
			CLK_COUNT_1MHZ <= X"00";
				CLK_1MHZ <= NOT(CLK_1MHZ);
			end if;
		else
			null;
		end if;
	end process;



	-----------------------------------------------------------------------------------------------
	-- Compute Total Number of microseconds for each experimental timing value.     --
	-----------------------------------------------------------------------------------------------
	OnDelay <=
conv_std_logic_vector(OnDelay_sec*1000000+OnDelay_msec*1000+OnDelay_usec,32);
	OffDelay <=
conv_std_logic_vector(OffDelay_sec*1000000+OffDelay_msec*1000+OffDelay_usec,32);
	OnPW <=
conv_std_logic_vector(OnPW_sec*1000000+OnPW_msec*1000+OnPW_usec,32);
	OffPW <=
conv_std_logic_vector(OffPW_sec*1000000+OffPW_msec*1000+OffPW_usec,32);

	-----------------------------------------------------------------------------------------------
	-- Check to see if the selected timing vales are valid.                                       --
	-- Check to see if experiment has finished.                                                   --
	-----------------------------------------------------------------------------------------------
	process (OnDelay, OffDelay, OnPW, OffPW, exp_Time)
	begin
		if (OnDelay + OnPW + X"FA" < OffDelay AND OffPW > X"00" AND OnPW >
X"00") then
			valid_timing <= '1';
		else
			valid_timing <= '0';
		end if;
```

```
        if (exp_Time < OnDelay + OffDelay + OnPW + OffPW + X"3E8") then
                end_experiment <= '0';
        else
                end_experiment <= '1';
        end if;
end process;

-------------------------------------------------------------------------------------------------
-- Converts Each Integer Value for Seconds, Milliseconds, and Microseconds to     --
-- three binary coded decimal digits.  Outputs the nine digits corresponding to the  --
-- selected time value along with the binary signals required by the LCD driver to   --
-- select the appropriate display screen.                                          --
-------------------------------------------------------------------------------------------------
process(current_display)
        variable s1, s2, s3, ms1, ms2, ms3, us1, us2, us3    :    integer range 0 to 9   := 0;
begin
        case current_display is
                when VALID_ENABLE =>
                        next_display <= DELAY_ON;
                when DELAY_ON =>
                        next_display <= PW_ON;
                        -- second digits --
                        s3 := OnDelay_sec / 100;
                        s2 := (OnDelay_sec mod 100)/10;
                        s1 := (OnDelay_sec mod 10);
                        -- millisecond digits --
                        ms3 := OnDelay_msec / 100;
                        ms2 := (OnDelay_msec mod 100)/10;
                        ms1 := (OnDelay_msec mod 10);
                        -- microsecond digits --
                        us3 := OnDelay_usec / 100;
                        us2 := (OnDelay_usec mod 100)/10;
                        us1 := (OnDelay_usec mod 10);
        -- Allows User to Modify the Timing Value for the On Pulse Delay --
                        case current_value is
                                when SEC =>
                                    OnDelay_sec <= conv_integer(switch(9 downto 0));
                                    next_value <= mSEC;
                                when mSEC =>
                                   OnDelay_msec <= conv_integer(switch(9 downto 0));
                                   next_value <= uSEC;
                                when uSEC =>
                                    OnDelay_usec <= conv_integer(switch(9 downto 0));
                                    next_value <= HOLD;
```

```
                        when HOLD =>
                            next_value <= SEC;
                end case;
        when PW_ON =>
                next_display <= DELAY_OFF;
                -- second digits --
                s3 := OnPW_sec / 100;
                s2 := (OnPW_sec mod 100)/10;
                s1 := (OnPW_sec mod 10);
                -- millisecond digits --
                ms3 := OnPW_msec / 100;
                ms2 := (OnPW_msec mod 100)/10;
                ms1 := (OnPW_msec mod 10);
                -- microsecond digits --
                us3 := OnPW_usec / 100;
                us2 := (OnPW_usec mod 100)/10;
                us1 := (OnPW_usec mod 10);
-- Allows User to Modify the Timing Value for the On Pulse Width --
                case current_value is
                        when SEC =>
                            OnPW_sec <= conv_integer(switch(9 downto 0));
                            next_value <= mSEC;
                        when mSEC =>
                            OnPW_msec <= conv_integer(switch(9 downto 0));
                            next_value <= uSEC;
                        when uSEC =>
                            OnPW_usec <= conv_integer(switch(9 downto 0));
                            next_value <= HOLD;
                        when HOLD =>
                            next_value <= SEC;
                end case;
        when DELAY_OFF =>
                next_display <= PW_OFF;
                -- second digits --
                s3 := OffDelay_sec / 100;
                s2 := (OffDelay_sec mod 100)/10;
                s1 := (OffDelay_sec mod 10);
                -- millisecond digits --
                ms3 := OffDelay_msec / 100;
                ms2 := (OffDelay_msec mod 100)/10;
                ms1 := (OffDelay_msec mod 10);
                -- microsecond digits --
                us3 := OffDelay_usec / 100;
                us2 := (OffDelay_usec mod 100)/10;
```

```
                us1 := (OffDelay_usec mod 10);
-- Allows User to Modify the Timing Value for the Off Pulse Delay --
                case current_value is
                        when SEC =>
                            OffDelay_sec <= conv_integer(switch(9 downto 0));
                            next_value <= mSEC;
                        when mSEC =>
                            OffDelay_msec <= conv_integer(switch(9 downto 0));
                            next_value <= uSEC;
                        when uSEC =>
                            OffDelay_usec <= conv_integer(switch(9 downto 0));
                            next_value <= HOLD;
                        when HOLD =>
                            next_value <= SEC;
                end case;
        when PW_OFF =>
                next_display <= VALID_ENABLE;
                -- second digits --
                s3 := OffPW_sec / 100;
                s2 := (OffPW_sec mod 100)/10;
                s1 := (OffPW_sec mod 10);
                -- millisecond digits --
                ms3 := OffPW_msec / 100;
                ms2 := (OffPW_msec mod 100)/10;
                ms1 := (OffPW_msec mod 10);
                -- microsecond digits --
                us3 := OffPW_usec / 100;
                us2 := (OffPW_usec mod 100)/10;
                us1 := (OffPW_usec mod 10);
-- Allows User to Modify the Timing Value for the Off Pulse Width --
                case current_value is
                        when SEC =>
                            OffPW_sec <= conv_integer(switch(9 downto 0));
                            next_value <= mSEC;
                        when mSEC =>
                            OffPW_msec <= conv_integer(switch(9 downto 0));
                            next_value <= uSEC;
                        when uSEC =>
                           OffPW_usec <= conv_integer(switch(9 downto 0));
                            next_value <= HOLD;
                        when HOLD =>
                            next_value <= SEC;
                end case;
end case;
```

```
		-- Display All Nine Digits --
		if (s3 > 9 OR s2 > 9 OR s1 > 9 OR ms3 > 9 OR ms2 > 9 OR ms1 > 9 OR us3 > 9
OR us2 > 9 OR us1 > 9) then
			secHundred <= X"F";
			secTen <= X"F";
			secOne <= X"F";
			millisecHundred <= X"F";
			millisecTen <= X"F";
			millisecOne <= X"F";
			microsecHundred <= X"F";
			microsecTen <= X"F";
			microsecOne <= X"F";
		else
			secHundred <= conv_std_logic_vector(s3,4);
			secTen <= conv_std_logic_vector(s2,4);
			secOne <= conv_std_logic_vector(s1,4);
			millisecHundred <= conv_std_logic_vector(ms3,4);
			millisecTen <= conv_std_logic_vector(ms2,4);
			millisecOne <= conv_std_logic_vector(ms1,4);
			microsecHundred <= conv_std_logic_vector(us3,4);
			microsecTen <= conv_std_logic_vector(us2,4);
			microsecOne <= conv_std_logic_vector(us1,4);
		end if;
	end process;



	-------------------------------------------------------------------------------------------------
	-- Indicates which value is currently being set by the bank of toggle switches.		--
	-- Displays " SEC" when the switches are used to modify the seconds value.  Displays	--
	-- "nSEC" when the switches are used to modify the millisecond value.  Displays		--
	-- "uSec" when the switches are used to modify the microsecond value.			--
	-------------------------------------------------------------------------------------------------
	process(current_value)
	begin
		case current_value is
			when SEC =>
				hex3 <= X"7F";			--	--
				hex2 <= X"12";			-- 'S' --
				hex1 <= X"06";			-- 'E' --
				hex0 <= X"46";			-- 'C' --
			when mSEC =>
			   hex3 <= X"2B";			-- 'm' --
```

```
                    hex2 <= X"12";          -- 'S' --
                    hex1 <= X"06";          -- 'E' --
                    hex0 <= X"46";          -- 'C' --
                when uSEC =>
                  hex3 <= X"63";            -- 'u' --
                    hex2 <= X"12";          -- 'S' --
                    hex1 <= X"06";          -- 'E' --
                    hex0 <= X"46";          -- 'C' --
                when HOLD =>
                  hex3 <= X"3F";            --    --
                    hex2 <= X"3F";          --    --
                    hex1 <= X"3F";          --    --
                    hex0 <= X"3F";          --    --
        end case;
end process;



-------------------------------------------------------------------------------------------------
-- Sets values for all 32 digits of the LCD display based on the currently selected   --
-- display mode.  The function allows for five different display screens:             --
--              (1)  Check Timing and Experiment Enable                               --
--              (2)  On Pulse Delay                                                   --
--              (3)  On Pulse Width                                                   --
--              (4)  Off Pulse Delay                                                  --
--              (5)  Off Pulse Width                                                  --
-------------------------------------------------------------------------------------------------
process (current_display)
begin
        -- Indicates If Program Ready to Fire
        if (current_display = VALID_ENABLE) then
                -- LINE 1 --
                M1 <= "01010110";       --'V'
                M2 <= "01100001";       --'a'
                M3 <= "01101100";       --'l'
                M4 <= "01101001";       --'i'
                M5 <= "01100100";       --'d'
                M6 <= "00100000";
                M7 <= "01010100";       --'T'
                M8 <= "01101001";       --'i'
                M9 <= "01101101";       --'m'
                M10 <= "01101001";      --'i'
                M11 <= "01101110";      --'n'
                M12 <= "01100111";      --'g'
```

```
		M13 <= "00111010";		--':'
		M14 <= "00100000";
		if (valid_timing = '1') then
			M15 <= "01011001";	-- 'Y'
		else
			M15 <= "01001110";	-- 'N'
		end if;
		M16 <= "00100000";
		-- LINE 2 --
		M17 <= "01000110";		--'F'
		M18 <= "01101001";		--'i'
		M19 <= "01110010";		--'r'
		M20 <= "01100101";		--'e'
		M21 <= "00100000";
		M22 <= "01000101";		--'E'
		M23 <= "01101110";		--'n'
		M24 <= "01100001";		--'a'
		M25 <= "01100010";		--'b'
		M26 <= "01101100";		--'l'
		M27 <= "01100101";		--'e'
		M28 <= "00111010";		--':'
		M29 <= "00100000";
		if (system_enable = '1') then
			M30 <= "01011001";	-- 'Y'
		else
			M30 <= "01001110";	-- 'N'
		end if;
		M31 <= "00100000";
		M32 <= "00100000";
-- Displays Time Delay to Start of "Turn On" Pulse
 elsif (current_display = DELAY_ON) then
		-- LINE 1 --
		M1 <= "01010100";		--'T'
		M2 <= "01110101";		--'u'
		M3 <= "01110010";		--'r'
		M4 <= "01101110";		--'n'
		M5 <= "00100000";
		M6 <= "01001111";		--'O'
		M7 <= "01101110";		--'n'
		M8 <= "00100000";
		M9 <= "01000100";		--'D'
		M10 <= "01100101";		--'e'
		M11 <= "01101100";		--'l'
		M12 <= "01100001";		--'a'
```

```
            M13 <= "01111001";          --'y'
            M14 <= "00111010";          --':'
            M15 <= "00100000";
            M16 <= "00100000";
            -- LINE 2 --
            M17 <= "0011" & secHundred;
            M18 <= "0011" & secTen;
            M19 <= "0011" & secOne;
            M20 <= "01110011";          -- 's'
            M21 <= "00100000";
            M22 <= "0011" & millisecHundred;
            M23 <= "0011" & millisecTen;
            M24 <= "0011" & millisecOne;
            M25 <= "01101101";          -- 'm'
            M26 <= "01110011";          -- 's'
            M27 <= "00100000";
            M28 <= "0011" & microsecHundred;
            M29 <= "0011" & microsecTen;
            M30 <= "0011" & microsecOne;
            M31 <= "01110101";          -- 'u'
            M32 <= "01110011";          -- 's'
    -- Displays Pulse Width of "Turn On" Pulse
    elsif (current_display = PW_ON) then
            -- LINE 1 --
            M1 <= "01010000";           --'P'
            M2 <= "01110101";           --'u'
            M3 <= "01101100";           --'l'
            M4 <= "01110011";           --'s'
            M5 <= "01100101";           --'e'
            M6 <= "00100000";
            M7 <= "01010111";       --'W'
            M8 <= "01101001";           --'i'
            M9 <= "01100100";       --'d'
            M10 <= "01110100";          --'t'
            M11 <= "01101000";          --'h'
            M12 <= "00111010";          --':'
            M13 <= "00100000";
            M14 <= "01001111";          --'O'
            M15 <= "01101110";          --'n'
            M16 <= "00100000";
            -- LINE 2 --
            M17 <= "0011" & secHundred;
            M18 <= "0011" & secTen;
            M19 <= "0011" & secOne;
```

```
            M20 <= "01110011";          -- 's'
            M21 <= "00100000";
            M22 <= "0011" & millisecHundred;
            M23 <= "0011" & millisecTen;
            M24 <= "0011" & millisecOne;
            M25 <= "01101101";          -- 'm'
            M26 <= "01110011";          -- 's'
            M27 <= "00100000";
            M28 <= "0011" & microsecHundred;
            M29 <= "0011" & microsecTen;
            M30 <= "0011" & microsecOne;
            M31 <= "01110101";          -- 'u'
            M32 <= "01110011";          -- 's'
        -- Displays Time Delay to Start of "Turn Off" Pulse
         elsif (current_display = DELAY_OFF) then
            -- LINE 1 --
            M1 <= "01010100";           --'T'
            M2 <= "01110101";           --'u'
            M3 <= "01110010";           --'r'
            M4 <= "01101110";           --'n'
            M5 <= "00100000";
            M6 <= "01001111";           --'O'
            M7 <= "01100110";           --'f'
            M8 <= "01100110";           --'f'
            M9 <= "00100000";
            M10 <= "01000100";          --'D'
            M11 <= "01100101";          --'e'
            M12 <= "01101100";          --'l'
            M13 <= "01100001";          --'a'
            M14 <= "01111001";          --'y'
            M15 <= "00111010";          --':'
            M16 <= "00100000";
            -- LINE 2 --
            M17 <= "0011" & secHundred;
            M18 <= "0011" & secTen;
            M19 <= "0011" & secOne;
            M20 <= "01110011";          -- 's'
            M21 <= "00100000";
            M22 <= "0011" & millisecHundred;
            M23 <= "0011" & millisecTen;
            M24 <= "0011" & millisecOne;
            M25 <= "01101101";          -- 'm'
            M26 <= "01110011";          -- 's'
            M27 <= "00100000";
```

```
        M28 <= "0011" & microsecHundred;
        M29 <= "0011" & microsecTen;
        M30 <= "0011" & microsecOne;
        M31 <= "01110101";          -- 'u'
        M32 <= "01110011";          -- 's'
-- Displays Pulse Width of "Turn Off" Pulse
 elsif (current_display = PW_OFF) then
        -- LINE 1 --
        M1 <= "01010000";           --'P'
        M2 <= "01110101";           --'u'
        M3 <= "01101100";           --'l'
        M4 <= "01110011";           --'s'
        M5 <= "01100101";           --'e'
        M6 <= "00100000";
        M7 <= "01010111";       --'W'
        M8 <= "01101001";           --'i'
        M9 <= "01100100";       --'d'
        M10 <= "01110100";          --'t'
        M11 <= "01101000";          --'h'
        M12 <= "00111010";          --':'
        M13 <= "00100000";
        M14 <= "01001111";          --'O'
        M15 <= "01100110";          --'f'
        M16 <= "01100110";          --'f'
        -- LINE 2 --
        M17 <= "0011" & secHundred;
        M18 <= "0011" & secTen;
        M19 <= "0011" & secOne;
        M20 <= "01110011";          -- 's'
        M21 <= "00100000";
        M22 <= "0011" & millisecHundred;
        M23 <= "0011" & millisecTen;
        M24 <= "0011" & millisecOne;
        M25 <= "01101101";          -- 'm'
        M26 <= "01110011";          -- 's'
        M27 <= "00100000";
        M28 <= "0011" & microsecHundred;
        M29 <= "0011" & microsecTen;
        M30 <= "0011" & microsecOne;
        M31 <= "01110101";          -- 'u'
        M32 <= "01110011";          -- 's'
else
        null;
end if;
```

```
end process;
-------------------------------------------------------------------------------------------
-- Clock Divider: Generates a 1kHz 50% Duty Cycle Signal                    --
-------------------------------------------------------------------------------------------
process (CLOCK_50MHZ)
begin
        if (CLOCK_50MHZ'EVENT AND CLOCK_50MHZ = '1') then
                if (CLK_COUNT_1kHZ < X"061A8") then
                        CLK_COUNT_1kHZ <= CLK_COUNT_1kHZ + 1;
                else
                CLK_COUNT_1kHZ <= X"00000";
                        CLK_1kHZ <= NOT(CLK_1kHZ);
                end if;
        else
                null;
        end if;
end process;



-------------------------------------------------------------------------------------------
-- LCD Driver:  Writes All 32 Characters to the LCD Display                 --
-------------------------------------------------------------------------------------------
process (CLK_1kHZ)
begin
        if (CLK_1kHZ'EVENT AND CLK_1kHZ='1') then
                case current_LCD is
                        when RESET =>
                                LCD_EN <= '1';
                                LCD_RS <= '0';
                                LCD_RW <= '0';
                                LCD_DATA_VALUE <= X"38";
                                current_LCD <= TOGGLE_E;
                                next_LCD <= FUNC_SET;
                        when FUNC_SET =>
                                LCD_EN <= '1';
                                LCD_RS <= '0';
                                LCD_RW <= '0';
                                LCD_DATA_VALUE <= X"38";
                                current_LCD <= TOGGLE_E;
                                next_LCD <= DISPLAY_OFF;
                        when DISPLAY_OFF =>
                                LCD_EN <= '1';
                                LCD_RS <= '0';
```

```
            LCD_RW <= '0';
            LCD_DATA_VALUE <= X"08";
            current_LCD <= TOGGLE_E;
            next_LCD <= DISPLAY_CLEAR;
        when DISPLAY_CLEAR =>
            LCD_EN <= '1';
            LCD_RS <= '0';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= X"01";
            current_LCD <= TOGGLE_E;
            next_LCD <= DISPLAY_ON;
        when DISPLAY_ON =>
            LCD_EN <= '1';
            LCD_RS <= '0';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= X"0C";
            current_LCD <= TOGGLE_E;
            next_LCD <= FIRST_LINE_MODE;
        when FIRST_LINE_MODE =>
            LCD_EN <= '1';
            LCD_RS <= '0';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= X"06";
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR1;
        when CHAR1 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M1;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR2;
        when CHAR2 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M2;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR3;
        when CHAR3 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M3;
```

```
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR4;
        when CHAR4 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M4;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR5;
        when CHAR5 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M5;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR6;
        when CHAR6 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M6;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR7;
        when CHAR7 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M7;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR8;
        when CHAR8 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M8;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR9;
        when CHAR9 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M9;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR10;
```

```
when CHAR10 =>
        LCD_EN <= '1';
        LCD_RS <= '1';
        LCD_RW <= '0';
        LCD_DATA_VALUE <= M10;
        current_LCD <= TOGGLE_E;
        next_LCD <= CHAR11;
when CHAR11 =>
        LCD_EN <= '1';
        LCD_RS <= '1';
        LCD_RW <= '0';
        LCD_DATA_VALUE <= M11;
        current_LCD <= TOGGLE_E;
        next_LCD <= CHAR12;
when CHAR12 =>
        LCD_EN <= '1';
        LCD_RS <= '1';
        LCD_RW <= '0';
        LCD_DATA_VALUE <= M12;
        current_LCD <= TOGGLE_E;
        next_LCD <= CHAR13;
when CHAR13 =>
        LCD_EN <= '1';
        LCD_RS <= '1';
        LCD_RW <= '0';
        LCD_DATA_VALUE <= M13;
        current_LCD <= TOGGLE_E;
        next_LCD <= CHAR14;
when CHAR14 =>
        LCD_EN <= '1';
        LCD_RS <= '1';
        LCD_RW <= '0';
        LCD_DATA_VALUE <= M14;
        current_LCD <= TOGGLE_E;
        next_LCD <= CHAR15;
when CHAR15 =>
        LCD_EN <= '1';
        LCD_RS <= '1';
        LCD_RW <= '0';
        LCD_DATA_VALUE <= M15;
        current_LCD <= TOGGLE_E;
        next_LCD <= CHAR16;
when CHAR16 =>
        LCD_EN <= '1';
```

```
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M16;
            current_LCD <= TOGGLE_E;
            next_LCD <= NEW_LINE;
        when NEW_LINE =>
            LCD_EN <= '1';
            LCD_RS <= '0';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= X"C0";
            current_LCD <= TOGGLE_E;
            next_LCD <= SECOND_LINE_MODE;
        when SECOND_LINE_MODE =>
            LCD_EN <= '1';
            LCD_RS <= '0';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= X"06";
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR17;
        when CHAR17 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M17;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR18;
        when CHAR18 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M18;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR19;
        when CHAR19 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M19;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR20;
        when CHAR20 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
```

```
            LCD_DATA_VALUE <= M20;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR21;
        when CHAR21 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M21;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR22;
        when CHAR22 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M22;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR23;
        when CHAR23 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M23;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR24;
        when CHAR24 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M24;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR25;
        when CHAR25 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M25;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR26;
        when CHAR26 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M26;
            current_LCD <= TOGGLE_E;
```

```
            next_LCD <= CHAR27;
        when CHAR27 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M27;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR28;
        when CHAR28 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M28;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR29;
        when CHAR29 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M29;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR30;
        when CHAR30 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M30;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR31;
        when CHAR31 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M31;
            current_LCD <= TOGGLE_E;
            next_LCD <= CHAR32;
        when CHAR32 =>
            LCD_EN <= '1';
            LCD_RS <= '1';
            LCD_RW <= '0';
            LCD_DATA_VALUE <= M32;
            current_LCD <= TOGGLE_E;
            next_LCD <= RETURN_ORIGIN;
        when RETURN_ORIGIN =>
```

```
                                LCD_EN <= '1';
                                LCD_RS <= '0';
                                LCD_RW <= '0';
                                LCD_DATA_VALUE <= X"80";
                                current_LCD <= TOGGLE_E;
                                next_LCD <= FIRST_LINE_MODE;
                        when TOGGLE_E =>
                                LCD_EN <= '0';
                                current_LCD <= HOLD;
                        when HOLD =>
                                current_LCD <= next_LCD;
                end case;
        end if;
    end process;


    -- Set tri-state register of LCD_DATA for bidirecitonal bus --
    LCD_DATA <= LCD_DATA_VALUE WHEN LCD_RW = '0' ELSE "ZZZZZZZZ";
    -- Set LCD Display Power --
    LCD_ON <= '1';
    LCD_BLON <= '1';

    -- Set the tri-state register of GPIO for bidirectional bus --
    GPIO(0) <= '0';
    GPIO(1) <= Disable;
    GPIO(2) <= '0';
    GPIO(3) <= OnLow;
    GPIO(4) <= '0';
    GPIO(5) <= OffHigh;
    GPIO(6) <= '0';
    GPIO(7) <= OffLow;
    GPIO(8) <= '0';
    GPIO(9) <= OnHigh;
    GPIO(35 downto 10) <= "ZZZZZZZZZZZZZZZZZZZZZZZZZZ";

    -- Red LED outputs:  Toggle Switch Status --
    ledr(17 downto 16) <= switch(17 downto 16);
    ledr(15 downto 14) <= not switch(15 downto 14);
    ledr(13 downto 12) <= switch(13 downto 12);
    ledr(9 downto 0) <= switch(9 downto 0);

    -- Green LED outputs:          LCD Activity --
    ledg(7 downto 0) <= LCD_DATA_VALUE;
END logic;
```

APPENDIX C: DEVICE DATASHEETS

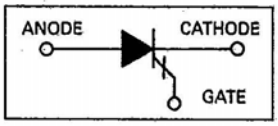
Gate Turn-Off Thyristors

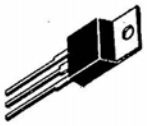
MGTO1000
MGTO1200

GTOs
18 AMPERES RMS
1000 and 1200 VOLTS

The GTO is a family of asymmetric gate turn-off thyristors designed primarily for dc power switching applications such as motor drives, switching power supplies, inverters, or wherever a need exists for high surge current capabilities and fast switching speeds.

- Fast Turn-Off With Reverse Gate Pulse
- High Voltage — V_{DRXM} = 1000 and 1200 Volts
- Momentary Forward Pulse For Turn-On
- Minimizes Drive Losses
- Interdigitated Emitter Geometry Aids Turn-On Current Spreading and Improves Turn-On di/dt
- Clip and Current Spreading Ring for Reliable High Surge Capability — I_{TSM} = 200 A





CASE 221A-04
(TO-220AB)
STYLE 3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage (T_J = −40 to +125°C, 1/2 Sine Wave 50 to 60 Hz) Note 1	V_{DRXM}	1000 1200	Volts
Repetitive Peak Reverse Voltage, Gate Open (T_J = −40 to +125°C), Note 2	V_{RRM}	15	Volts
Repetitive Peak Reverse Gate Voltage, Note 3	V_{GRM}	15	Volts
On-State Current at T_C = 65°C (1/2 Cycle Sine Wave, 50 to 60 Hz)	$I_{T(RMS)}$	18	Amps
Peak Nonrepetitive Surge Current (8.3 ms Conduction, Half Sine Wave T_C = 65°C)	I_{TSM}	200	Amps
Circuit Fusing (t = 8.3 ms)	I^2t	167	A^2s
Repetitive Controllable On-State Current, Note 4	I_{TCM}	50	Amps
Nonrepetitive Maximum Interruptable On-State Current, Note 5	I_{TCSM}	70	Amps
Peak Forward Gate Power	P_{GFM}	10	Watts
Average Forward Gate Power	$P_{GF(AV)}$	3	Watts
Peak Reverse Gate Power	P_{GRM}	400	Watts
Average Reverse Gate Power	$P_{GR(AV)}$	5	Watts
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

3

Notes: 1. V_{DRXM} for all types can be applied on a continuous basis without damage. Ratings apply for R = 39 Ω or shorted gate conditions or negative voltage on the gate. Devices should not be tested for blocking voltage such that the supply voltage exceeds the rating of the device.
2. This is an asymmetric anode shorted part with a blocking gate-cathode junction. The ability to support a reverse voltage depends on the gate-cathode terminal conditions. Gate-cathode reverse bias increases V_{RRM}.
3. Instantaneous voltage at turn-off may exceed rated V_{GRM} provided P_{GRM} is not exceeded.
4. V_D Maximum Peak = V_{DRXM} − 300 V, T_J < 125°C, L_G = 2 μH, V_{GR} = 12 V (See Figure 2)
   C_S = 0.1 μF for MGTO1000
   C_S = 0.05 μF for MGTO1200
5. V_D Maximum Peak = V_{DRXM} − 300 V, T_J < 125°C, L_G = 2 μH, V_{GR} = 12 V (See Figure 2)
   C_S = 0.2 μF for MGTO1000
   C_S = 0.1 μF for MGTO1200

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted), Note 1

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (V_D = Rated V_{DRM}, R_{GK} = 39 Ω, T_J = 125°C)	I_{DRM}	—	—	5	mA
Peak On-State Voltage (I_{TM} = 50 A, Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%, I_{GT} = 300 mAdc)	V_{TM}	—	2.7	3.1	Volts
Peak Gate Trigger Current (V_D = 12 Vdc, R_L = 1.4 Ω, Pulse Width ≥ 10 μs)	I_{GTM}	—	60	300	mA
Peak Gate Trigger Voltage (V_D = 12 Vdc, R_L = 1.4 Ω, Pulse Width ≥ 10 μs)	V_{GTM}	—	0.8	1.5	Volts
Reverse Gate Leakage Current (V_{GRM} = 15 V, T_J = 125°C)	I_{GRM}	—	—	5	mA
Latching Current (PW = 300 μs, f = 60 Hz, Gate Pulse = 1 A, 10 μs, V_D = 12 Vdc)	I_L	—	1	—	Adc
Holding Current (PW = 300 μs, f = 60 Hz, Gate Pulse = 1 A, 10 μs, Anode Pulse = 6 A, 100 μs, V_D = 12 Vdc)	I_H	—	700	—	mA

SWITCHING CHARACTERISTICS (T_J = 25°C unless otherwise noted)

RESISTIVE TURN-ON SWITCHING						
Gate Turn-On Time	V_D = 600 V, I_T = 50 A $I_{G(pk)}$ = 6 A, C_S = 0.1 μF dig/dt ≥ 7 A/μs See Figure 1 and Table 1(A)	t_{gt}	—	1.5	—	μs
Turn-On Delay Time		t_{dl}	—	0.6	—	
Rise Time		t_{ri}	—	0.9	—	
INDUCTIVE TURN-OFF SWITCHING						
Gate Tun-Off Time	$V_{D(pk)}$ = 700 V, I_T = 50 A, V_{GR} = 12 V $I_{G(pk)}$ = 6 A L_G = 2 μH, C_S = 0.1 μF See Figure 2 and Table 1(B)	t_{gq}	—	3	—	μs
Storage Time		T_{si}	—	2.6	—	
Fall Time		T_{fi}	—	0.4	—	
GATE TURN-OFF CHARGE						
Gate Charge	$V_{D(pk)}$ = 700 V, I_T = 50 A V_{GR} = 12 V L_G = 2 μH, C_S = 0.1 μF See Table 1(B)	Q_{GQ}	—	35	—	μC
Peak Reverse Gate Current		I_{GQ}	—	17	—	
Peak Tail Current		I_{TLP}	—	5	—	A
STATIC dv/dt						
Critical Exponent of Rise Time	$V_{(pk)} = V_{DRM}$ − 400 V R_{GK} = 39 Ω, T_J = 125°C Linear Waveform	dv/dt	—	10,000	—	V/μs

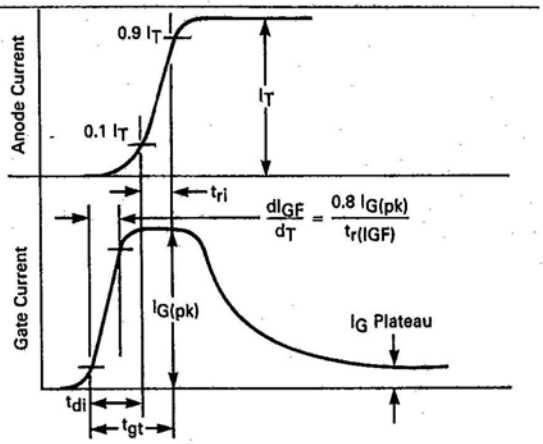
Note 1. This device is rated for use in applications subject to high surge conditions. Care must be taken to insure proper heat-sinking is used at sustained currents (see derating curves).

3

TABLE 1 — TERMS, SYMBOLS AND DEFINITIONS FOR SWITCHING WITH GTO'S

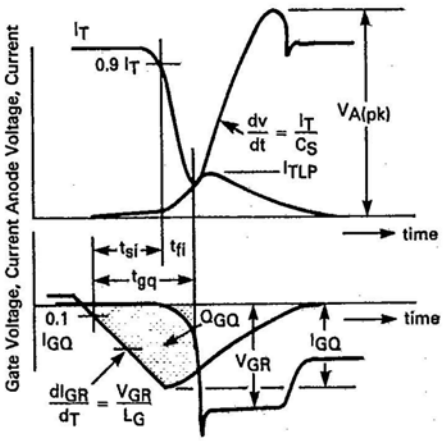
NOTE: The parameters are shown on two separate graphs for clarity.

Terms	Symbols	Definitions
RESISTIVE TURN-ON SWITCHING		
Turn-On Time	t_{gt}	
Delay Time	t_{di}	
Rise Time	t_{ri}	



(A)

INDUCTIVE TURN-OFF SWITCHING		
Gate Controlled Turn-Off Time	t_{gq}	
Current Storage Time	t_{si}	
Current Fall Time	t_{fi}	
Turn-Off Gate Charge	Q_{GQ}	
Peak Tail Current	I_{TLP}	



(B)

t_{si} — current storage time 10% I_{GR} to 90% I_T
t_{fi} — current fall time 90% I_T to I_{TLP} Inflection point
t_{gq} — gate controlled turn-off time (t_{si} + t_{fi})
t_{di} — current delay time. 10% $I_{G(pk)}$ to 10% I_T
t_{ri} — current rise time. 10% I_T to 90% I_T
t_{gt} — turn-on time (t_{di} + t_{ri})

3

International
IOR Rectifier

PD - 95361

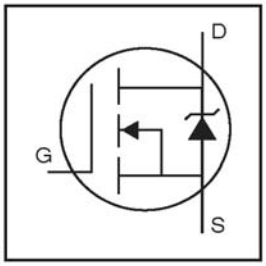
AUTOMOTIVE MOSFET

IRF1010ZPbF
IRF1010ZSPbF
IRF1010ZLPbF

HEXFET® Power MOSFET

Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free



V_{DSS} = 55V

$R_{DS(on)}$ = 7.5mΩ

I_D = 75A

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating . These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

TO-220AB IRF1010Z | D²Pak IRF1010ZS | TO-262 IRF1010ZL

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	94	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	66	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	75	
I_{DM}	Pulsed Drain Current ①	360	
P_D @T_C = 25°C	Power Dissipation	140	W
	Linear Derating Factor	0.90	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy②	130	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ⑥	180	
I_{AR}	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw ⑦	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.11	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface ⑦	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ⑦	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑧	—	40	

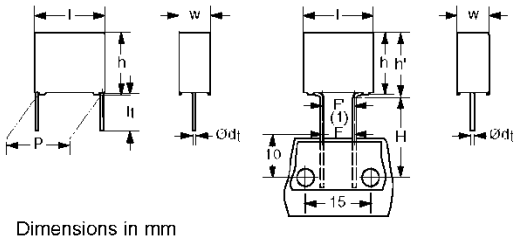
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.049	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	5.8	7.5	mΩ	V_{GS} = 10V, I_D = 75A ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
gfs	Forward Transconductance	33	—	—	S	V_{DS} = 25V, I_D = 75A
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 55V, V_{GS} = 0V
		—	—	250		V_{DS} = 55V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -20V
Q_g	Total Gate Charge	—	63	95		I_D = 75A
Q_{gs}	Gate-to-Source Charge	—	19	—	nC	V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	24	—		V_{GS} = 10V ③
$t_{d(on)}$	Turn-On Delay Time	—	18	—		V_{DD} = 28V
t_r	Rise Time	—	150	—		I_D = 75A
$t_{d(off)}$	Turn-Off Delay Time	—	36	—	ns	R_G = 6.8 Ω
t_f	Fall Time	—	92	—		V_{GS} = 10V ③
L_D	Internal Drain Inductance	—	4.5	—		Between lead,
					nH	6mm (0.25in.)
L_S	Internal Source Inductance	—	7.5	—		from package
						and center of die contact
C_{iss}	Input Capacitance	—	2840	—		V_{GS} = 0V
C_{oss}	Output Capacitance	—	420	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	250	—	pF	f = 1.0MHz
C_{oss}	Output Capacitance	—	1630	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	360	—		V_{GS} = 0V, V_{DS} = 44V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	—	560	—		V_{GS} = 0V, V_{DS} = 0V to 44V ④

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current	—	—	75		MOSFET symbol
	(Body Diode)				A	showing the
I_{SM}	Pulsed Source Current	—	—	360		integral reverse
	(Body Diode) ①					p-n junction diode.
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 75A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	22	33	ns	T_J = 25°C, I_F = 75A, V_{DD} = 25V
Q_{rr}	Reverse Recovery Charge	—	15	23	nC	di/dt = 100A/µs ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

AC and Pulse Double Metallized Polypropylene Film Capacitors
MMKP Radial Potted Type



Dimensions in mm
(1) |F – F'| < 0.3 mm
F = 7.5 – 0.6/– 0.1 mm

APPLICATIONS

Where steep pulses occur e.g. SMPS (switch mode power supplies). Electronic lighting e.g. Ballast. Motor control circuits. S - correction. For flyback applications please use 1400 V series. For hot asphalt encapsulation process.

MARKING

C-value; tolerance; rated voltage; code for dielectric material; code for factory of origin; manufacturer's type designation; manufacturer; year and week of manufacture

DIELECTRIC

Polypropylene film

ELECTRODES

Metallized film

ENCAPSULATION

Flame retardant plastic case and epoxy resin (UL-class 94 V-0)

CONSTRUCTION

Internal serial construction

LEADS

Tinned wire

CAPACITANCE RANGE (E24 SERIES):

0.001 to 2.7 µF

CAPACITANCE TOLERANCE:

± 5 %

FEATURES

7.5 mm bent back pitch. 15 to 27.5 mm lead pitch. Low contact resistance. Low loss dielectric. Small dimensions for high density packaging. Supplied loose in box and taped on reel

Lead (Pb)-free product

RoHS-compliant product

RoHS COMPLIANT

RATED (DC) VOLTAGE

250 V; 400 V; 630 V; 1000 V; 1400 V;1600 V; 2000 V; 2500 V

RATED (AC) VOLTAGE

125 V; 200 V; 220 V; 350 V; 500 V; 550 V; 700 V; 900 V

RATED PEAK-TO-PEAK VOLTAGE

350 V; 560 V; 630 V; 1000 V; 1400 V; 1600 V; 2000 V; 2500 V

CLIMATIC CATEGORY

55/105/56

RATED (DC) TEMPERATURE

85 °C

RATED (AC) TEMPERATURE

105 °C

MAXIMUM APPLICATION TEMPERATURE

105 °C

REFERENCE SPECIFICATIONS

IEC 60384-17

PERFORMANCE GRADE

Grade 1 (long life)

STABILITY GRADE

Grade 2

DETAIL SPECIFICATION

For more detailed data and test requirements contact: filmcaps.roeselare@vishay.com

SPECIFIC REFERENCE DATA (1000 VDC)

DESCRIPTION	VALUE	
Tangent of loss angle:	at 10 kHz	at 100 kHz
$C \leq 0.062\ \mu F$	$\leq 5 \times 10^{-4}$	$\leq 15 \times 10^{-4}$
$0.062\ \mu F < C \leq 0.13\ \mu F$	$\leq 6 \times 10^{-4}$	$\leq 20 \times 10^{-4}$
$0.13\ \mu F < C \leq 0.22\ \mu F$	$\leq 8 \times 10^{-4}$	$\leq 25 \times 10^{-4}$
$0.22\ \mu F < C \leq 0.33\ \mu F$	$\leq 8 \times 10^{-4}$	$\leq 30 \times 10^{-4}$
$0.33\ \mu F < C \leq 0.47\ \mu F$	$\leq 8 \times 10^{-4}$	$\leq 35 \times 10^{-4}$
Rated voltage pulse slope $(dU/dt)_R$:		
P = 15.0 mm and 7.5 mm (bent back), $C \leq 0.024\ \mu F$	1700 V/µs	
P = 15.0 mm and 7.5 mm (bent back), $0.024\ \mu F < C \leq 0.062\ \mu F$	3300 V/µs	
P = 22.5 mm	1200 V/µs	
P = 27.5 mm, for $0.13\ \mu F < C \leq 0.33\ \mu F$	700 V/µs	
P = 27.5 mm, for $0.33\ \mu F < C \leq 0.47\ \mu F$	470 V/µs	
R between leads, for $C \leq 1\ \mu F$ at 500 V; 1 minute	> 100000 MΩ	
R between leads and case; 500 V; 1 minute	> 30000 MΩ	
Ionization (AC) voltage (typical value) at 50 pC peak discharge	> 440 V	
Withstanding (DC) voltage (cut off current 10 mA); rise time 100 V/s	1600 V; 1 minute	
Withstanding (DC) voltage between leads and case	2840 V; 1 minute	

U_{Rdc} = 1000 V; U_{Rac} = 350 V/$U_{p\text{-}p}$ = 1000 V

C (µF)	DIMENSIONS w × h (h') × l (mm)	MASS (g)	CATALOG NUMBER 2222 383 ..... AND PACKAGING						
			LOOSE IN BOX			REEL			
			lt = 3.5 ± 0.3 mm	SHORT LEADS	LONG LEADS	ORIGINAL PITCH	PITCH = 7.5 mm (BENT BACK)		
			C-tol = ± 5 %				C-tol = ± 5 %		
							∅ 500 mm		∅ 356 mm
			LAST 5 DIGITS OF CATALOG NUMBER	SPQ	SPQ	SPQ	LAST 5 DIGITS OF CATALOG NUMBER	SPQ	SPQ
Pitch = 15.0 ± 0.4 mm; d_t = 0.80 ± 0.08 mm						pitch = 15.0 mm	pitch = 7.5 mm (bent back)		
0.0043	5.0 × 11.0 (13.0) × 17.5	1.2	30432	1250	1000	1100	33432	950	550
0.0047			30472				33472		
0.0051			30512				33512		
0.0056			30562				33562		
0.0062			30622				33622		
0.0068			30682				33682		
0.0075			30752				33752		
0.0082			30822				33822		
0.0091			30912				33912		
0.010			30103				33103		
0.011			30113				33113		
0.012			30123				33123		
0.013			30133				33133		
0.015			30153				33153		
0.016			30163				33163		
0.018	6.0 × 12.0 (14.0) × 17.5	1.5	30183	1000	1000	900	33183	800	450
0.02			30203				33203		
0.022			30223				33223		
0.024			30243				33243		
0.027	7.0 × 13.5 (15.5) × 17.5	2.0	30273	750	500	800	33273	700	400
0.03			30303				33303		
0.033			30333				33333		

MMKP 383

Vishay BCcomponents

AC and Pulse Double Metallized
Polypropylene Film Capacitors
MMKP Radial Potted Type

C (µF)	DIMENSIONS w × h (h') × l (mm)	MASS (g)	CATALOG NUMBER 2222 383 ..... AND PACKAGING					
			LOOSE IN BOX			REEL		
			lt = 3.5 ± 0.3 mm	SHORT LEADS	LONG LEADS	ORIGINAL PITCH	PITCH = 7.5 mm (BENT BACK)	
			C-tol = ± 5 %				C-tol = ± 5 %	
							∅ 500 mm	∅ 356 mm
			LAST 5 DIGITS OF CATALOG NUMBER	SPQ	SPQ	SPQ	LAST 5 DIGITS OF CATALOG NUMBER	SPQ	SPQ
0.036	8.5 × 15.0 (17.0) × 17.5	2.7	30363	750	500	650	33363	550	300
0.039			30393				33393		
0.043			30433				33433		
0.047			30473				33473		
0.051	10.0 × 16.5 (18.5) × 17.5	3.3	30513	500	450	600	33513	500	250
0.056			30563				33563		
0.062			30623				33623		
Pitch = 22.5 ± 0.4 mm; d_t = 0.80 ± 0.08 mm						pitch = 22.5 mm	pitch = 7.5 mm (bent back)		
0.068	7.0 × 16.5 × 26.0	3.5	30683	200	250	550			
0.075	8.5 × 18.0 × 26.0	4.8	30753	200	250	450			
0.082			30823						
0.091			30913						
0.1	10.0 × 19.5 × 26.0	6.0	30104	200	200	350			
0.11			30114						
0.12			30124						
0.13			30134						
Pitch = 27.5 ± 0.4 mm; d_t = 0.80 ± 0.08 mm						pitch = 27.5 mm	pitch = 7.5 mm (bent back)		
0.15	11.0 × 21.0 × 31.0	8.4	30154	100	125				
0.16			30164						
0.18			30184						
0.2	13.0 × 23.0 × 31.0	11.0	30204	100	125				
0.22			30224						
0.24			30244						
0.27	15.0 × 25.0 × 31.0	13.6	30274	100	125				
0.3			30304						
0.33			30334						
0.36	18.0 × 28.0 × 31.0	18.5	30364	100	100				
0.39			30394						
0.43			30434						
0.47			30474						

FAIRCHILD SEMICONDUCTOR®

RURG8060

Data Sheet **January 2002**

80A, 600V Ultrafast Diode

The RURG8060 is an ultrafast diode with soft recovery characteristics (t_{rr} < 75ns). It has low forward voltage drop and is of silicon nitride passivated ion-implanted epitaxial planar construction.

This device is intended for use as a freewheeling/clamping diode and rectifier in a variety of switching power supplies and other power switching applications. Its low stored charge and ultrafast recovery with soft recovery characteristic minimize ringing and electrical noise in many power switching circuits, thus reducing power loss in the switching transistors.

Formerly developmental type TA09886.

Ordering Information

PART NUMBER	PACKAGE	BRAND
RURG8060	TO-247	RURG8060

NOTE: When ordering, use the entire part number.

Symbol

Features

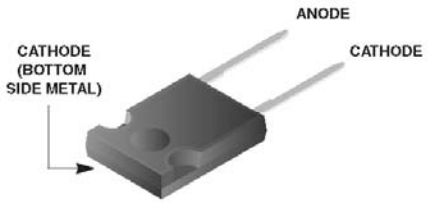
- Ultrafast with Soft Recovery . . . . . <75ns
- Operating Temperature . . . . . 175°C
- Reverse Voltage 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Packaging

JEDEC STYLE 2 LEAD TO-247



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RURG8060	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	600	V
Working Peak Reverse Voltage	V_{RWM}	600	V
DC Blocking Voltage	V_R	600	V
Average Rectified Forward Current ($T_C = 72^oC$)	$I_{F(AV)}$	80	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FRM}	160	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	800	A
Maximum Power Dissipation	P_D	180	W
Avalanche Energy (See Figures 7 and 8)	E_{AVL}	50	mJ
Operating and Storage Temperature	T_{STG}, T_J	-65 to 175	°C

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
V_F	$I_F = 80A$	-	-	1.6	V
	$I_F = 80A$, $T_C = 150^oC$	-	-	1.4	V
I_R	$V_R = 600V$	-	-	250	μA
	$V_R = 600V$, $T_C = 150^oC$	-	-	2.0	mA
t_{rr}	$I_F = 1A$, $dI_F/dt = 100A/\mu s$	-	-	75	ns
	$I_F = 80A$, $dI_F/dt = 100A/\mu s$	-	-	85	ns
t_a	$I_F = 80A$, $dI_F/dt = 100A/\mu s$	-	40	-	ns
t_b	$I_F = 80A$, $dI_F/dt = 100A/\mu s$	-	25	-	ns
$R_{\theta JC}$		-	-	0.83	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{rr} = Reverse recovery time (See Figure 6), summation of $t_a + t_b$.

t_a = Time to reach peak reverse current (See Figure 6).

t_b = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 6).

$R_{\theta JC}$ = Thermal resistance junction to case.

pw = pulse width.

D = duty cycle.

Typical Performance Curves

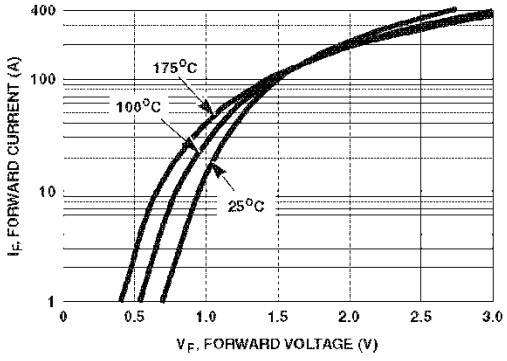


FIGURE 1. FORWARD CURRENT vs FORWARD VOLTAGE

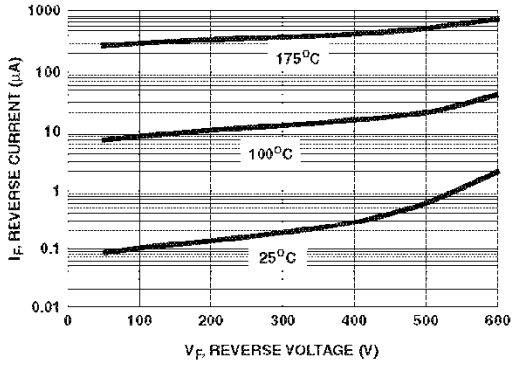


FIGURE 2. REVERSE CURRENT vs REVERSE VOLTAGE

Data Sheet | January 3, 2006 | FN3676.4

80V, 1.25A Peak Current H-Bridge FET Driver

The HIP4082 is a medium frequency, medium voltage H-Bridge N-Channel MOSFET driver IC, available in 16 lead plastic SOIC (N) and DIP packages.

Specifically targeted for PWM motor control and UPS applications, bridge based designs are made simple and flexible with the HIP4082 H-bridge driver. With operation up to 80V, the device is best suited to applications of moderate power levels.

Similar to the HIP4081, it has a flexible input protocol for driving every possible switch combination except those which would cause a shoot-through condition. The HIP4082's reduced drive current allows smaller packaging and it has a much wider range of programmable dead times (0.1 to 4.5µs) making it ideal for switching frequencies up to 200kHz. The HIP4082 does not contain an internal charge pump, but does incorporate non-latching level-shift translation control of the upper drive circuits.

This set of features and specifications is optimized for applications where size and cost are important. For applications needing higher drive capability the HIP4080A and HIP4081A are recommended.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HIP4082IB*	HIP4082IB	-55 to +125	16 Ld SOIC (N)	M16.15
HIP4082IBZ* (Note)	4082IBZ	-55 to +125	16 Ld SOIC (N) (Pb-free)	M16.15
HIP4082IP	HIP4082IP	-55 to +125	16 Ld PDIP	E16.3
HIP4082IPZ (Note)	HIP4082IPZ	-55 to +125	16 Ld PDIP** (Pb-free)	E16.3

*Add "-T" suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

**Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Features

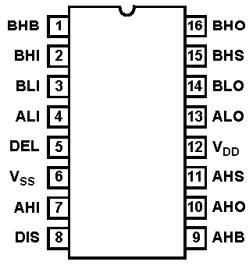
- Independently Drives 4 N-Channel FET in Half Bridge or Full Bridge Configurations
- Bootstrap Supply Max Voltage to 95VDC
- Drives 1000pF Load in Free Air at 50°C with Rise and Fall Times of Typically 15ns
- User-Programmable Dead Time (0.1 to 4.5µs)
- DIS (Disable) Overrides Input Control and Refreshes Bootstrap Capacitor when Pulled Low
- Input Logic Thresholds Compatible with 5V to 15V Logic Levels
- Shoot-Through Protection
- Undervoltage Protection
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

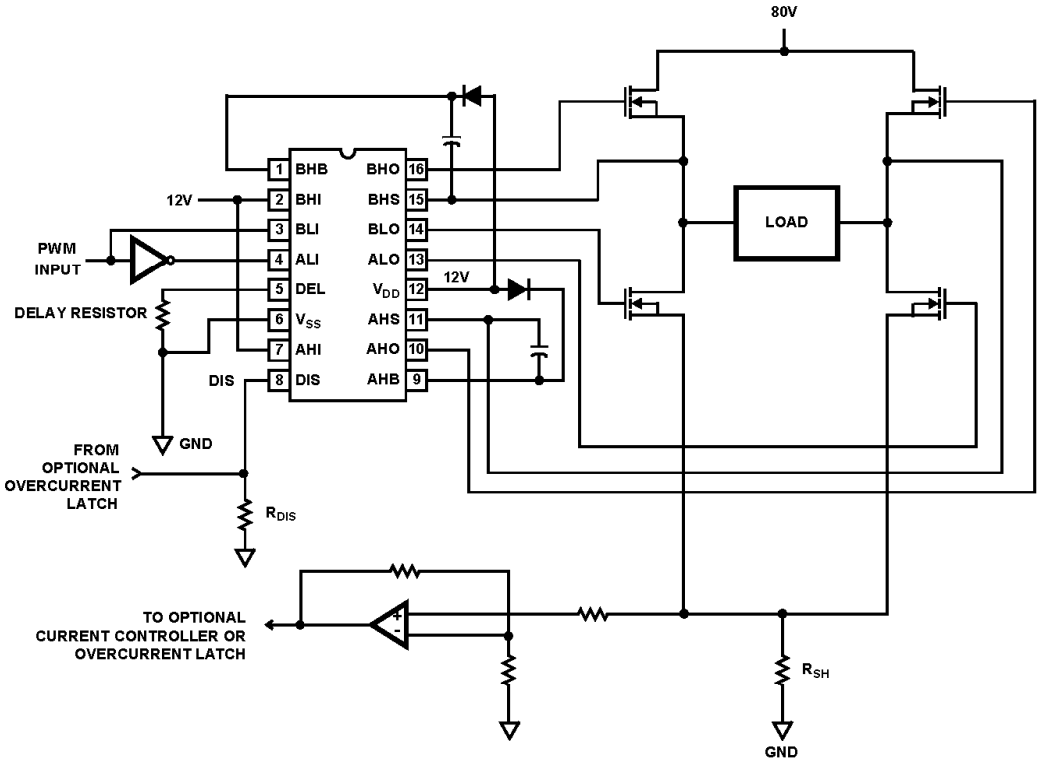
- UPS Systems
- DC Motor Controls
- Full Bridge Power Supplies
- Switching Power Amplifiers
- Noise Cancellation Systems
- Battery Powered Vehicles
- Peripherals
- Medium/Large Voice Coil Motors
- Related Literature
  - TB363, Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)

Pinout

HIP4082
(PDIP, SOIC)
TOP VIEW



Typical Application (PWM Mode Switching)



Absolute Maximum Ratings

Supply Voltage, V_{DD} . . . . . -0.3V to 16V
Logic I/O Voltages . . . . . -0.3V to V_{DD} +0.3V
Voltage on AHS, BHS . . . . . -6V (Transient) to 80V (25°C to 150°C)
Voltage on AHS, BHS . . . . . -6V (Transient) to 70V (-55°C to150°C)
Voltage on AHB, BHB . . . . . $V_{AHS, BHS}$ -0.3V to $V_{AHS, BHS}$ +V_{DD}
Voltage on ALO, BLO. . . . . V_{SS} -0.3V to V_{DD} +0.3V
Voltage on AHO, BHO . . . $V_{AHS, BHS}$ -0.3V to $V_{AHB, BHB}$ +0.3V Input
Current, DEL . . . . . -5mA to 0mA
Phase Slew Rate 20V/ns
NOTE: All voltages are relative V_{SS} unless otherwise specified.

Operating Conditions

Supply Voltage, V_{DD} . . . . . +8.5V to +15V
Voltage on V_{SS}. . . . . -1.0V to +1.0V
Voltage on AHB, BHB . . . . . $V_{AHS, BHS}$ +7.5V to $V_{AHS, BHS}$ +V_{DD}
Input Current, DEL . . . . . -4mA to -100µA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)
SOIC Package	115
DIP Package	90

Maximum Power Dissipation. . . . . See Curve
Storage Temperature Range . . . . . -65°C to +150°C
Operating Max. Junction Temperature. . . . . +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C
(For SOIC - Lead Tips Only))

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V_{DD} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{AHS} = V_{BHS} = 0V$, $R_{DEL} = 100K$

PARAMETER	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -55°C TO +150°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
SUPPLY CURRENTS & UNDER VOLTAGE PROTECTION								
V_{DD} Quiescent Current	I_{DD}	All inputs = 0V, R_{DEL} = 100K	1.2	2.3	3.5	0.85	4	mA
		All inputs = 0V, R_{DEL} = 10K	2.2	4.0	5.5	1.9	6.0	mA
V_{DD} Operating Current	I_{DDO}	f = 50kHz, no load	1.5	2.6	4.0	1.1	4.2	mA
		50kHz, no load, R_{DEL} = 10kΩ	2.5	4.0	6.4	2.1	6.6	mA
AHB, BHB Off Quiescent Current	I_{AHBL}, I_{BHBL}	AHI = BHI = 0V	0.5	1.0	1.5	0.4	1.6	mA
AHB, BHB On Quiescent Current	I_{AHBH}, I_{BHBH}	AHI = BHI = V_{DD}	65	145	240	40	250	µA
AHB, BHB Operating Current	I_{AHBO}, I_{BHBO}	f = 50kHz, CL = 1000pF	.65	1.1	1.8	.45	2.0	mA
AHS, BHS Leakage Current	I_{HLK}	$V_{AHS} = V_{BHS}$ = 80V $V_{AHB} = V_{BHB}$ = 96 V_{DD} = Not Connected	-	-	1.0	-	-	µA
V_{DD} Rising Undervoltage Threshold	V_{DDUV+}		6.8	7.6	8.25	6.5	8.5	V
V_{DD} Falling Undervoltage Threshold	V_{DDUV-}		6.5	7.1	7.8	6.25	8.1	V
Undervoltage Hysteresis	UVHYS		0.17	0.4	0.75	0.15	0.90	V
AHB, BHB Undervoltage Threshold	VHBUV	Referenced to AHS & BHS	5	6.0	7	4.5	7.5	V
INPUT PINS: ALI, BLI, AHI, BHI, & DIS								
Low Level Input Voltage	V_{IL}	Full Operating Conditions	-	-	1.0	-	0.8	V
High Level Input Voltage	V_{IH}	Full Operating Conditions	2.5	-	-	2.7		V
Input Voltage Hysteresis			-	35	-	-	-	mV
Low Level Input Current	I_{IL}	V_{IN} = 0V, Full Operating Conditions	-145	-100	-60	-150	-50	µA
High Level Input Current	I_{IH}	V_{IN} = 5V, Full Operating Conditions	-1	-	+1	-10	+10	µA
TURN-ON DELAY PIN DEL								
Dead Time	T_{DEAD}	R_{DEL} = 100K	2.5	4.5	8.0	2.0	8.5	µs
		R_{DEL} = 10K	0.27	0.5	0.75	0.2	0.85	µs

Electrical Specifications $V_{DD} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{AHS} = V_{BHS} = 0V$, $R_{DEL} = 100K$ **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -55°C TO +150°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
GATE DRIVER OUTPUT PINS: ALO, BLO, AHO, & BHO								
Low Level Output Voltage	V_{OL}	I_{OUT} = 50mA	0.65		1.1	0.5	1.2	V
High Level Output Voltage	V_{DD}-V_{OH}	I_{OUT} = -50mA	0.7		1.2	0.5	1.3	V
Peak Pullup Current	I_O+	V_{OUT} = 0V	1.1	1.4	2.5	0.85	2.75	A
Peak Pulldown Current	I_O-	V_{OUT} = 12V	1.0	1.3	2.3	0.75	2.5	A

Switching Specifications $V_{DD} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{AHS} = V_{BHS} = 0V$, R_{DEL}= 100K, C_L = 1000pF.

PARAMETER	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -55°C TO +150°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
Lower Turn-off Propagation Delay (ALI-ALO, BLI-BLO)	T_{LPHL}		-	25	50	-	70	ns
Upper Turn-off Propagation Delay (AHI-AHO, BHI-BHO)	T_{HPHL}		-	55	80	-	100	ns
Lower Turn-on Propagation Delay (ALI-ALO, BLI-BLO)	T_{LPLH}		-	40	85	-	100	ns
Upper Turn-on Propagation Delay (AHI-AHO, BHI-BHO)	T_{HPLH}		-	75	110	-	150	ns
Rise Time	T_R		-	9	20	-	25	ns
Fall Time	T_F		-	9	20	-	25	ns
Minimum Input Pulse Width	$T_{PWIN-ON/OFF}$		50	-	-	50	-	ns
Output Pulse Response to 50 ns Input Pulse	T_{PWOUT}			63			80	ns
Disable Turn-off Propagation Delay (DIS - Lower Outputs)	T_{DISLOW}		-	50	80	-	90	ns
Disable Turn-off Propagation Delay (DIS - Upper Outputs)	$T_{DISHIGH}$		-	75	100	-	125	ns
Disable Turn-on Propagation Delay (DIS - ALO & BLO)	T_{DLPLH}		-	40	70	-	100	ns
Disable Turn-on Propagation Delay (DIS- AHO & BHO)	T_{DHPLH}	R_{DEL} = 10K	-	1.2	2	-	3	µs
Refresh Pulse Width (ALO & BLO)	T_{REF-PW}		375	580	900	350	950	ns

TRUTH TABLE

INPUT					OUTPUT	
ALI, BLI	AHI, BHI	VDDUV	VHBUV	DIS	ALO, BLO	AHO, BHO
X	X	X	X	1	0	0
X	X	1	X	X	0	0
0	X	0	1	0	0	0
1	X	0	X	0	1	0
0	1	0	0	0	0	1
0	0	0	0	0	0	0

NOTE: X signifies that input can be either a "1" or "0".

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	BHB	B High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin.
2	BHI	B High-side Input. Logic level input that controls BHO driver (Pin 16). BLI (Pin 3) high level input overrides BHI high level input to prevent half-bridge shoot-through, see Truth Table. DIS (Pin 8) high level input overrides BHI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
3	BLI	B Low-side Input. Logic level input that controls BLO driver (Pin 14). If BHI (Pin 2) is driven high or not connected externally then BLI controls both BLO and BHO drivers, with dead time set by delay currents at DEL (Pin 5). DIS (Pin 8) high level input overrides BLI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
4	ALI	A Low-side Input. Logic level input that controls ALO driver (Pin 13). If AHI (Pin 7) is driven high or not connected externally then ALI controls both ALO and AHO drivers, with dead time set by delay currents at DEL (Pin 5). DIS (Pin 8) high level input overrides ALI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
5	DEL	Turn-on DELay. Connect resistor from this pin to V_{SS} to set timing current that defines the dead time between drivers. All drivers turn-off with no adjustable delay, so the DEL resistor guarantees no shoot-through by delaying the turn-on of all drivers. The voltage across the DEL resistor is approximately Vdd -2V.
6	V_{SS}	Chip negative supply, generally will be ground.
7	AHI	A High-side Input. Logic level input that controls AHO driver (Pin 10). ALI (Pin 4) high level input overrides AHI high level input to prevent half-bridge shoot-through, see Truth Table. DIS (Pin 8) high level input overrides AHI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
8	DIS	DISable input. Logic level input that when taken high sets all four outputs low. DIS high overrides all other inputs. When DIS is taken low the outputs are controlled by the other inputs. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
9	AHB	A High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin.
10	AHO	A High-side Output. Connect to gate of A High-side power MOSFET.
11	AHS	A High-side Source connection. Connect to source of A High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
12	V_{DD}	Positive supply to control logic and lower gate drivers. De-couple this pin to V_{SS} (Pin 6).
13	ALO	A Low-side Output. Connect to gate of A Low-side power MOSFET.
14	BLO	B Low-side Output. Connect to gate of B Low-side power MOSFET.
15	BHS	B High-side Source connection. Connect to source of B High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
16	BHO	B High-side Output. Connect to gate of B High-side power MOSFET.

APPENDIX D: MATLAB SCRIPT (DATA ANALYSIS)

```
function [Ia_r,Ig_max,Q_startV,Rgate,t_Vrise,t_Ifall,dVdt,dIdt] = GenerateTraces(filename)

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%  TRIDENT EXPERIMENT DATA ANALYSIS SCRIPT                                        %
%                                                                                 %
%  Organization:  United States Navy                                              %
%  Location:        United States Naval Academy                                   %
%                                                                                 %
%  Author:    MIDN Gerald E. Vineyard USN                                         %
%  Data:       5 March 2008                                                       %
%                                                                                 %
%  Measured Values:                                                               %
%     CH1 - Anode to Cathode Current       - Rogowski Coil                        %
%     CH2 - Anode to Cathode Voltage       - Differential Voltage Probe           %
%     CH3 - Gate to Cathode Current        - Rogowski Coil                        %
%     CH4 - Gate to Cathode Voltage        - Differential Voltage Probe           %
%                                                                                 %
%                                                                                 %
% [Ia_r,Ig_max,Q_startV,Rgate,t_Vrise,t_Ifall,dVdt,dIdt] = GenerateTraces(filename)  %
%                                                                                 %
%     GenerateTrace(filename) – Extracts data from an excel spreadsheet containing %
%     the numerical output of the oscilloscope.  "filename" specifies the name of the %
%     Excel spreadsheet to analyze.                                               %
%                                                                                 %
%     The function generates plots of the voltage and current waveforms and computes %
%     the anode blocking current as measured by the rogowski coil (Ia_r).         %
%                                                                                 %
%     The function computes the maximum gate current Ig_max and the total gate    %
%     charge, Q_off, removed from the gate terminal during switch turn-off.       %
%                                                                                 %
%     The function computes the voltage rise time, t_Vrise, the current fall time, t_Ifall, %
%     the rate of voltage rise, dVdt, and rate of current fall, dIdt, in the anode-cathode %
%     path during switch turn-off.                                                %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


% SENSOR CALIBRATION COEFFICIENTS
coeff1 = 1;        %A/A_probe  - CH1
coeff2 = 500;      %V/V_probe  - CH2
coeff3 = 1;        %A/A_probe  - CH3
coeff4 = 50;       %V/V_probe  - CH4
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%                                    Import Data                                 %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
S = importdata([filename,'.xls']);

%Strip Out Individual Data Channels
CH1 = struct('time',S.data(:,3),'value',S.data(:,4));
CH2 = struct('time',S.data(:,9),'value',S.data(:,10));
CH3 = struct('time',S.data(:,15),'value',S.data(:,16));
CH4 = struct('time',S.data(:,21),'value',S.data(:,22));

%Check for Invalid Numbers and Replace with Zero Values
CH1.value(isnan(CH1.value)) = 0;
CH2.value(isnan(CH2.value)) = 0;
CH3.value(isnan(CH3.value)) = 0;
CH4.value(isnan(CH4.value)) = 0;

%Create General Time Vectors for The Two Sets of Data (CH1-CH4 and CH5-CH6)
time1 = CH1.time;
dt1 = S.data(2,1);



%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%          Smooth out Waveforms and Scale to Correct Voltage/Current Range      %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
smooth = [.25,.25,.25,.25];                 % Anode Current
Ia_rog = conv(CH1.value,smooth)*coeff1;      % Smooth and Scale
Ia_rog = Ia_rog(1:length(time1));           % Truncate to Original Length

smooth = [0.25,0.25,0.25,0.25];             % Anode Voltage
Va_rog = conv(CH2.value,smooth)*coeff2;     % Smooth and Scale
Va_rog = Va_rog(1:length(time1));           % Truncate to Original Length

smooth = [.333,.333,.333];                  % Gate Current
Igate = conv(CH3.value,smooth)*coeff3;      % Smooth and Scale
Igate = Igate(1:length(time1));             % Truncate to Original Length

smooth = [.333,.333,.333];                   % Gate Voltage
Vgate = conv(CH4.value,smooth)*coeff4;      % Smooth and Scale
Vgate = Vgate(1:length(time1));             % Truncate to Original Length
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%                          Compute Maximum Gate Current                          %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Ig_max = max(Igate);        % Compute Maximum Gate Turn-Off Current



%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%                          Compute Gate Resistance                          %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Rgate = Vgate(find(Igate == max(Igate)))/max(Igate);
Rgate = Rgate(1);



%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%                          Compute Anode Current at Turn-off  (Ia_r)                          %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
IaON = mean(Ia_rog(find(Va_rog <= 0.05*max(Va_rog) & Va_rog >= 0.02*max(Va_rog))));
IaOFF = mean(Ia_rog(find(Va_rog >= 0.9*Va_rog(end) & Va_rog <= 1.1*Va_rog(end) &
abs(Ia_rog - min(Ia_rog)) < 0.2*(max(Ia_rog) - min(Ia_rog)))));

Ia_r = IaON - IaOFF;



%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%                          Compute Anode Current Fall Time (t_Ifall)                          %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Find Time to Maximum Current (Always Preceeds Turn-Off Transient)
t_Imax = time1(find(Ia_rog == max(Ia_rog)));
t_Imax = t_Imax(end);

% Extract all time values corresponding to the current turn-off transition
t_transition = time1(find(Ia_rog <= IaOFF+0.9*Ia_r & Ia_rog >= IaOFF+0.1*Ia_r & time1 >=
t_Imax));
t_startI = t_transition(1);
t_stopI = t_transition(end);

t_Ifall = length(t_transition)*dt1;        % Compute Current Fall Time (90% of initial to 10% of
initial)
dIdt = -0.8*Ia_r/t_Ifall;          % Compute Rate of Current Fall
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%                    Compute Anode Voltage Rise Time (t_Vrise)                    %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Determine average anode-cathod voltage for the switch on and off states
VaON = mean(Va_rog(find(Va_rog <= 0.05*max(Va_rog) & Va_rog >= 0.02*max(Va_rog))));
% On-state Anode Voltage
VaOFF = mean(Va_rog(find(Va_rog >= 0.98*max(Va_rog))));                  % Off-state
Anode Voltage
Va_r = VaOFF - VaON;         % Net Change in Anode-Cathode Voltage

% Determine Time to Maximum Voltage (Corresponds to Switch Fully Off)
t_Vmax = time1(find(Va_rog == max(Va_rog)));
t_Vmax = t_Vmax(1);

% Extract all time values corresponding to the voltage turn-off transient
t_transition = time1(find(Va_rog >= VaON+0.1*Va_r & Va_rog <= VaON+0.9*Va_r & time1
<= t_Vmax));     %Extract all time values durning current turn-off transition
t_startV = t_transition(1);
t_stopV = t_transition(end);

t_Vrise = length(t_transition)*dt1;          % Compute Voltage Rise Time (10% of final to 90%
of final)
dVdt = 0.8*Va_r/t_Vrise;             % Compute Rate of Voltage Rise



%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%                    Compute Turn-off Gate Charge (Qgate)                    %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Determine Start and Stop of Gate Turn-off Current Pulse (Start of Voltage Rise)
t_startG = time1(1);                    % Begining of Pulse
t_stopG = t_startV;                     % End of Pulse
buffer = (t_stopG - t_startG)*.20;          % 20% Integration Buffer

% Integrate current values with respect to time to compute total gate charge
Q_startV = sum(Igate(find(time1 >= t_startG & time1 < t_stopG+buffer))*dt1);
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%                       Display Results                %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
h1 = figure(1);
subplot(3,1,1)
plot(time1,Ia_rog,'k',[time1(1),time1(end)],[IaON, IaON],'b',[time1(1),time1(end)],[IaOFF,
IaOFF],'b',[t_startI,t_startI],[IaON,IaOFF],'r',[t_stopI,t_stopI],[IaON,IaOFF],'r')
xlabel('time - s')
ylabel('Current - A')
title(['Sequence - ',filename, '  Anode Current'])
grid on
axis([time1(1),time1(end),1.2*min(Ia_rog),1.2*max(Ia_rog)])
subplot(3,1,2)
plot(time1,Va_rog,'k',[time1(1),time1(end)],[VaON,VaON],'b',[time1(1),time1(end)],[VaOFF,V
aOFF],'b',[t_startV,t_startV],[VaON,VaOFF],'r',[t_stopV,t_stopV],[VaON,VaOFF],'r')
xlabel('time - s')
ylabel('Voltage - V')
title(['Sequence - ',filename, '  Anode Voltage'])
grid on
axis([time1(1),time1(end),min(Va_rog)-10,1.2*max(Va_rog)])
subplot(3,1,3)
plot(time1,Igate,'k',[time1(1),time1(end)],[Ig_max, Ig_max],'b',[time1(1),time1(end)],[0,
0],'b',[t_startG,t_startG],[Ig_max,0],'r',[t_stopG,t_stopG],[Ig_max,0],'r')
xlabel('time - s')
ylabel('Current - A')
title(['Sequence - ',filename, '  Gate Current'])
grid on
axis([time1(1),time1(end),1.2*min(Igate),1.2*max(Igate)])

h2 = figure(2);
plot(time1,Ia_rog,'m',time1,Va_rog,'b',time1,Igate,'k',time1,Vgate,'g')
grid on
xlabel('time - s')
title(['Sequence - ',filename])
axis tight

saveas(h1,[filename,'a.fig']);
saveas(h2,[filename,'b.fig']);
```

REFERENCES

[1] United States Naval Research Advisory Committee Panel on Electromagnetic (EM) Gun Technology Assessment, Electromagnetic (EM) Gun Technology Assessment, (Office of the Assistant Secretary of the Navy - Research, Development, and Acquisition), 2004.

[2] T. Erline, L. Fisher, Rapid Assessment of Small Changes to Major Gun and Projectile Dynamic Parameters, (Army Research Laboratory - Aberdeen Proving Grounds, Maryland), 1997.

[3] J. Hartke, Characterization and Magnetic Augmentation of a Low Voltage Electromagnetic Railgun, (Naval Postgraduate School, Montery, California), 1997.

[4] A. Sitzman, D. Surls, J. Mallick, Stretch Meatgrinder: A Novel Circuit Toplogy for Reducing Opening Switch Voltage Stress, (Institute for Advance Technology – University of Texas, Texas), 2007.

[5] A. Sitzman, D. Surls, J. Mallick, Modification and Testing of a Battery-Inductor Repetitive Pulse Power Supply for a Small Railgun, (Institute for Advanced Technology, University of Texas at Austin), 2007

[6] Mitsubishi Electric, Mitsubishi High Power Semiconductors: Feature and Application of Gate Turn Off Thyristors, (Mitsubishi Electric), 1998.

[7] N. Galster, S. Klaka, A. Weber, Thyristor Product Design Guide: Section 2, (ABB Semiconductors, Zurich, Switzerland), 2007.

[8] N, Galster, S. Klaka, A. Wever, Thyristor Product Design Guide: Section 5, (ABB Semiconductors, Zurich, Switzerland), 2007.

[9] N. Galster, S. Klaka, A. Weber, Thyristor Product Design Guide: Section 2, (ABB Semiconductors, Zurich, Switzerland), 2007.

[10] E. Ho and P. Sen, Effect of Gate-Drive Circuits on GTO Thyristor Characteristics, (Queen's University, Kinston, Ontario, Canada), 1986.

[11] P. Hoban, M. Rahimo, and N. Shammas, Electrical Transients of Snubber Diodes in GTO Circuits, (Saffordshire University, U.K.), 1993.

[12] Mitsubishi Electric, Mitsubishi High Power Semiconductors: Feature and Application of Gate Turn Off Thyristors, (Mitsubishi Electric), 1998.

[13] G. Skibinski, D. Divan, GTO Characterization for Zero Voltage Switching Applications, (University of Wisconsin, Madison, Wisconsin), 1991.

[14] Mitsubishi Electric, Mitsubishi High Power Semiconductors: Feature and Application of Gate Turn Off Thyristors, (Mitsubishi Electric), 1998.

[15] A. Sitzman, D. Surls, J. Mallick, Modification and Testing of a Battery-Inductor Repetitive Pulse Power Supply for a Small Railgun, (Institute for Advanced Technology, University of Texas at Austin), 2007

[16] M. Kanter, et. all, Multikilojoule Inductive Modulator with Solid-State Opening Switches, (Propulsion Physics Laboratory - Soreq Nuclear Research Center, Yavana, Israel), 1992.

[17] J. Schwartzenberg, C. Tsay, and R. Fischl, A SPICE Model for Gate Turn-Off Thyristors, (Drexel University, Philidelphia, PA), 1990.

[18] O. Despe, J. Wang, Design of a Gate-Turn-Off (GTO) Switch for Pulsed Power Application, (Argonne National Laboratory, Argonne, Illinois), 1995.

[19] A. Huang, K. Motto, Y. Li, Development and Comparison of High-Power Semiconductor Switches, (Center for Power Electronic Systems, Virginia Polytechnic Institute and State University), 2000.

[20] E. Ho and P. Sen, Effect of Gate-Drive Circuits on GTO Thyristor Characteristics, (Department of Electrical Engineering, Queen's University in Kingston, Ontario), 1985.

[21] J. Hartke, Characterization and Magnetic Augmentation of a Low Voltage Electromagnetic Railgun, (Naval Postgraduate School, Monterey, California), 1997.

[22] A. Sitzman, D. Surls, J. Mallick, STRETCH Meat Grinder: A Novel Circuit Topology for Reducing Opening Switch Voltage Stress, (Institute for Advanced Technology, University of Texas at Austin), 2005.

[23] Internal Publication NSWC Dahlgren, MICROCAP circuit simulation of EMLF Launcher and Green Farm Capacitor Bank, (Electromagnetic Launch Facility, Naval Surface Warfare Center Dahlgren Division, Dahlgren, Virginia), 2007.

[24] Internal Publication IAT-UT, Design Specifications for MEL IPPS, (Institute for Advanced Technology, University of Texas at Austin), 2007.